REMARKS

CLAIM AMENDMENTS

CLAIM 1

Claim 1 is amended to specifically state how the devices are interconnected. Support for the amendments is provided by the original claim, Figs. 1-5, and paragraphs 44-47 of the specification. No new matter has been added.

CLAIMS 2-4

Names of quantities used in claims 2-4 have been changed in order to be consistent with the changes in claim 1.

CLAIM 32

The wording has been changed in order to remedy problems identified by the examiner.

CLAIM 41

Claim 41 is amended to specifically state how the devices are interconnected. Support for the amendments is provided by the original claim, Figs. 1, 12-17, and paragraphs 95-100 of the specification. No new matter has been added.

CLAIMS 42-46

Names of quantities used in claims 42-46 have been changed in order to be consistent with the changes in claim 41.

CLAIM 52

Claim 52 is amended to correct an error in the original claim.

CLAIM 72

The wording has been changed in order to remedy problems identified by the examiner.

DRAWINGS

The examiner's objection to the "transformer" feature of claim 40 not being shown in a drawing has been rectified by adding a phrase in the specification which points out that the transformers are like the ones shown in Figs. 3 and 4.

I. WHETHER CLAIMS 20-24 ARE UNPATENTABLE UNDER 35 U.S.C. § 112, FIRST PARAGRAPH, AS CONTAINING SUBJECT MATTER WHICH WAS NOT DESCRIBED IN THE SPECIFICATION IN SUCH A WAY AS TO REASONABLY CONVEY TO ONE SKILLED IN THE RELEVANT ART THAT THE INVENTOR(S), AT THE TIME THE APPLICATION WAS FILED, HAD POSSESSION OF THE CLAIMED INVENTION.

Applicants have shown possession of the claimed invention by describing a generic correlation detection system for identifying a received bit.

The technology which provides the basis of the resonance-tracking demodulator 15 in the reader (Fig. 1) is described in numerous textbooks and handbooks. The means for identifying a received bit (Claim 19) is a correlation detector system consisting of balanced mixers 81 and 82 and sampled integrators 83 and 84 in Fig. 6 and the corresponding devices in Fig. 7. The balanced mixers provide the means for multiplying an amplitude-demodulated received signal with zero-phase, zero-average square wave C_{cm0} or C_{cm1} reference signals. Specification, paragraphs 0058, 0059. The sampled integrators provide the integration means required in a correlation detector system.

A person skilled in the art would recognize that weighted integrations (as in claims 20-22) might be desirable for the purpose of suppressing intersymbol interference and the incorporation of such weights in the C_{cm0} or C_{cm1} reference signals is easily accomplished when the signals are generated by the VCO/CGC 13 (Fig. 1). This process, often referred to as "windowing", is also described in numerous textbooks and handbooks (see Attachment I, *Electronics Engineers' Handbook, Fourth Edition*, McGraw-Hill, New York, N.Y., 1997).

The examiner points out that the specification does not describe the specific weighted integrations claimed. Since specific weighting functions have been described, analyzed, and discussed extensively in the literature (see Attachment II, *The Industrial Electronics Handbook, IEEE Press*, 91-92, CRC Press LLC, Boca Raton, FL, 1997), it should not be necessary to repeat this material in the specification.

The examiner responded to the above arguments by stating:

"The applicants' conclusion is incorrect. All claimed subject matter must be supported by the disclosure" 08/12/03 Office Action, p. 11.

The examiner's statement is not supported by case law as reported in the Manual of Patent Examining Procedure:

> **"What is conventional or well known to one of ordinary skill in the art need not be disclosed in detail. See *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d at 1367, 1384, 231 USPQ 81, 94, (Fed. Cir. 1986). If a skilled artisan would have understood the inventor to be in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate description requirement is met." MPEP § 2163, II, A, 3, a.**

II. WHETHER CLAIMS 32-35 ARE UNPATENTABLE UNDER 35 U.S.C. § 112, SECOND PARAGRAPH, AS BEING INDEFINITE FOR FAILING TO PARTICULARLY POINT OUT AND DISTINCTLY CLAIM THE SUBJECT MATTER WHICH APPLICANTS REGARD AS THE INVENTION.

Claim 32 reads as follows:

32. (currently amended) A reader for use with a tag that ~~communicates~~ transmits a data sequence to the reader by repeating a message a plurality of times, the message comprising a preamble ~~consisting of a sync sequence of S bits~~, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, the tag data group and the error-detecting group possibly including false-sync sequences, the reader comprising:

a means for receiving the data sequence transmitted by the tag;

a means for detecting each sync sequence in the received data sequence;

a means for identifying the preamble;

a means for extracting the tag data group from the received data sequence utilizing the identification of the preamble.

The problems pointed out by the examiner have been rectified by the amendments to the claim.

III. WHETHER CLAIMS 32 AND 72 ARE UNPATENTABLE UNDER 35 U.S.C. § 102(B) AS BEING ANTICIPATED BY WARAKSA (U.S. 4,942,393).

Claim 32 reads as follows:

32. (currently amended) A reader for use with a tag that transmits a data sequence to the

reader by repeating a message a plurality of times, ***[1] the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, [2] the tag data group and the error-detecting group possibly including false-sync sequences,*** *the reader comprising:*

[3] a means for receiving the data sequence transmitted by the tag;

[4] a means for detecting each sync sequence in the received data sequence;

[5] a means for identifying the preamble;

[6] a means for extracting the tag data group from the received data sequence utilizing the identification of the preamble.

The limitations shown in bold face are not disclosed by Waraksa et al..

Limitation [1]

Claim 32 claims a reader which obtains data from a tag in the form of a message consisting of a plurality of bits, some of which constitute a "sync sequence" (limitation [1]). A "bit" is an abbreviation of "binary digit" and takes on one of two values, usually denoted as "0" or "1".

The communication of message bits from a tag to a reader requires the transformation of the message bits into analog waveforms that can be propagated electromagnetically by means of a carrier wave:

> "The terminology 'line coding' originated in telephony with the need to transmit digital information across a copper telephone *line*; more specifically, binary data over a digital repeatered line. The concept of line coding, however readily applies to any transmission line or channel. In a digital communication system, there exists a known set of symbols to be transmitted. These can be designated as $\{m_i\}$, $i=1, 2, \ldots, N$, with a probability of occurrence $\{p_i\}$, $i=1, 2, \ldots, N$, where the sequentially transmitted symbols are generally assumed to be statistically independent. The conversion or *coding* of these abstract symbols

into real, temporal waveforms to be transmitted in baseband is the process of line coding." The Communications Handbook, Editor-in-Chief Jerry D. Gibson, CRC Press, Inc. Boca Raton, FL (1987) p. 386.

The most common transformation is to associate each bit in a message with one of two distinguishable analog waveforms, a "0" bit being associated with a "0" waveform and a "1" bit being associated with a "1" waveform. To receive the data sequence transmitted by a tag using the "0" and "1" waveforms, the reader must perform the inverse transformation by identifying the appropriate bit value to be associated with each of the received analog waveforms.

For example, let us assume that the "0" waveform is a constant voltage V_0 for the bit period and the "1" waveform is a constant voltage V_1 for the bit period. The transformation of the message bits into bit waveforms by the tag and the reverse transformation of the received bit waveforms into received message bits by the reader is very straightforward. It is so straightforward, in fact, that a person skilled in the art may feel it unnecessary to distinguish between bits and bit waveforms, referring to either a bit or its associated bit waveform as a bit. Since a bit and its associated bit waveform are in a one-to-one relationship, why not refer to either as being a "0" or a "1"? In many cases this short-hand way of referring to either a bit or its associated waveform is harmless. However, consider another example.

Again assume that the "0" waveform is a constant voltage V_0 for the bit period and the "1" waveform is a constant voltage V_1 for the bit period. In addition, after the bit waveforms have been joined together into a message waveform, assume a "sync" waveform is added to the front end of the assembled message waveform by the tag to enable the reader to readily identify the beginning of a message waveform. And assume the "sync" waveform is a constant voltage V_0 maintained for the first half of a bit period and a constant voltage V_1 maintained for the second half of the bit period.

Note that the "sync" waveform is neither a "0" waveform nor a "1" waveform. It cannot be identified with either of the two bit values.

Waraksa et al., the prior art that the examiner asserts anticipates applicants' claim-32 invention, constitutes a second example of a "sync" waveform joined to a message waveform where the "sync" waveform cannot be transformed into a bit or a bit sequence.

Limitation [1] specifies that a "message" be comprised of a "preamble" (consisting of a sync sequence of S bits), a tag data group of T bits, and an error-detecting group of E bits. Waraksa et al. discloses a "message" consisting of a 4- bit function code, a 20-bit identification code, and a 24-bit error correction code. Waraksa et al., col. 8, lines 46-58. Waraksa et al.'s "message" does not include a preamble consisting of a sync sequence and thus, does not disclose one of the limitations of claim 32.

After line coding the "message" using the Miller line code (*id.* at 395), Waraksa et al. adds a special line code (illegal under Miller line coding) to the beginning of the Miller encoded "message". Waraksa et al., col. 9, lines 52-55. The Miller waveforms associated with various bit combinations are shown in Fig. 3 of Waraksa et al.

The examiner argues that "Waraksa et al. discloses an S-bit sync sequence in the preamble as claimed." 08/12/03 Office Action, p. 12. As pointed out above, Waraksa et al.'s "SYNC pattern" is an illegal Miller line code that is added to Waraksa et al.'s Miller encoded data word. Waraksa et al., col. 9, lines 34-36. Waraksa et al.'s "data word" corresponds to the claim-32 "message" and does not include a sync sequence. Waraksa et al.'s "data word" only contains a 4-bit function code, a 20-bit identification code, and a 24-bit ECC code. Waraksa et al., col. 9, lines 40-55.

The examiner argues that this preamble limitation can be ignored because "the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. 08/12/03 Office Action, p. 13. The examiner is incorrect. The body limitations utilize terms which are defined by the preamble limitations, and the preamble limitations cannot be ignored for this reason alone. Limitation [1] also limits the scope of claim 32 to messages containing a sync sequence, a tag data group, and an error-detecting group.

Limitation [2]

As claim 32 specifies, the tag repeats a message a number of times. A reader, when it starts receiving the message, does not know where the message begins. The sync sequence typically appears as the message preamble and thereby provides the means for the reader to identify the beginning of a message. There is a problem, however, in that the particular sequence chosen as the sync sequence may also appear by happenstance in the tag data group - error-correcting group portion of the message giving rise to a "false-sync" sequence and an erroneous indication of the beginning of the message. Thus, it is necessary to be able to distinguish in some fashion a "false-sync" sequence from the "sync sequence" that constitutes the message preamble. Limitation [2] points out the "false-sync" possibility, and the necessity for the claimed apparatus being capable of recognizing a "false-sync" when it occurs.

Waraksa et al. uses a sync line code that is not a proper Miller line code and consequently avoids the possibility of the Miller line codes for a 4-bit sequence in the "message" producing a false sync:

> "As previously noted, it is necessary for the receiver to identify the beginning of the encoded transmission word and for this purpose a 4-bit SYNC pattern is added at the beginning of the

code word which presents an illegal pattern for Miller encoding. Because of this illegal nature of the SYNC pattern, it can always be differentiated by the receiver from the code word." Waraksa et al., col. 6, line 66 - col. 7, line 4.

Note that the term "4-bit SYNC pattern" denotes a "SYNC pattern" that extends over a time period equivalent to that required to transmit the 4 Miller line codes for 4 "message" bits. Since the SYNC pattern is "an illegal pattern for Miller encoding", it cannot be transformed into the equivalent of 4 "message" bits.

Waraksa et al. does not disclose limitation [2] of claim 32.

The examiner argues that this preamble limitation can be ignored because "the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. 08/12/03 Office Action, p. 13. The examiner is incorrect. The possibility of the tag data group and the error-detecting group including false-sync sequences is the only reason for including limitations [4] and [5] in the claim.

The examiner also argues that the occurrence of false-sync sequences in the tag data group and the error-detecting group is specified as only a possibility, "and as such is not interpreted as a positive limitation." 08/12/03 Office Action, pp. 12-13. The examiner is incorrect. The limitation is a substantive one in that it requires that there be no constraints on the tag data group and the error-detecting group that would prevent the chance occurrence of false-sync sequences.

Limitation [3]

Limitation [3] specifies "a means for receiving the data sequence transmitted by the tag. The term "the data sequence transmitted by the tag" is defined in the preamble as a repeated message, "the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T

bits, and an error-detecting group of E bits." Thus, "the data sequence transmitted by the tag" includes "a sync sequence of S bits."

The first definition of "receive" is "to have (something) given or conferred on one." *The Random House College Dictionary Revised Edition*, Random House, Inc., New York, N.Y., 1988. Thus, "receiving the data sequence transmitted by the tag" means "to have the data sequence transmitted by the tag given or conferred on one." The term "data sequence" does not mean "line code modulated signals." Nor does it mean "line codes." The term "data sequence" means exactly what the preamble says it means: a repeated message, "the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group."

Waraksa et al. discloses "receiving" data from a beacon by decoding the Miller encoded data. Waraksa et al., col. 17, lines 24-34. The Miller encoded data is a transform of a "data word" into Miller line codes, the "data word" consisting of a 24-bit MESSAGE and a 24-bit ECC code. Waraksa et al., col. 9, lines 29-39. There are no sync bits in Waraksa et al.'s "data word." Waraksa et al.'s SYNC pattern (an illegal Miller line code) is added later to the line codes associated with the "data word". Waraksa et al., col. 9, lines 34-36.

Since Waraksa et al.'s received "data word" does not contain "a sync sequence of S bits", Waraksa et al. does not disclose limitation [3], a means for receiving a repeated message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits.

The examiner argues that limitation [3] "does not set forth receiving sync data bits." 08/12/03 Office Action, p. 13. However, the limitation states "a means for receiving the data

sequence transmitted by the tag" and "the data sequence transmitted by the tag" includes a sync sequence of S bits as stated in the preamble of the claim.

The examiner also argues that Waraksa et al. discloses receiving the Miller encoded code word and thereby discloses limitation [3], "receiving the data sequence transmitted by the tag." 08/12/03 Office Action, p. 13. As we pointed out above, "data sequence" in claim 32 corresponds to Waraksa et al.'s "code word" (Waraksa et al., col. 9, line 50). The "Miller encoded code word" are the joined-together line codes associated with the bits of the "code word". Thus, Waraksa et al.'s disclosure of receiving Miller encoded code words is not a disclosure of receiving Waraksa et al.'s "code word" or applicants' "data sequence".

Limitation [4]

Since Waraksa et al. does not disclose receiving a data sequence (Waraksa et al.'s "data word") that includes a sync sequence of S bits (see discussion under the ***Limitation [3]*** heading), Waraksa et al. obviously does not disclose limitation [4], "a means for detecting each sync sequence in the received data sequence."

The examiner argues: "The claim limitation is that the reader detects each sync sequence. Since the reader of Waraksa must detect the sync sequence in order for proper operation of the system, it reads on the claim." 08/12/03 Office Action, p. 14. The examiner omits five very important words (shown in boldface) in limitation [4]: "a means for detecting each sync sequence **in the received data sequence**." There is no sync sequence in Waraksa et al.'s received data sequence (see discussion under the ***Limitation [3]*** heading), and consequently, it would have been pointless for Waraksa et al. to include a means in their invention to detect such sequences.

Limitation [5]

Because applicants' "data sequence" may contain several "sync sequences"—the "sync sequence" which is the "preamble" and possibly one or more "false-sync sequences" that occur in the tag data group and the error-detecting group. In order to identify the tag data group and the error-detecting group, one must identify which of the "sync sequences" detected by the limitation [4] means is the "preamble".

Since Waraksa et al. does not disclose receiving a data sequence (Waraksa et al.'s "data word") containing a message having a preamble consisting of a sync sequence of S bits (see discussion under the ***Limitation [3]*** heading), Waraksa et al. obviously does not disclose limitation [5], "a means for identifying the preamble."

The examiner argues that:

"The preamble of Waraksa includes the sync sequence. Because Waraksa detects the sync sequence, the preamble is identified." 08/12/03 Office Action, p. 14.

Waraksa et al. discloses a 48-bit "code word" consisting of a 4-bit function code, a 20-bit identification code, and 24 parity bits. Waraksa et al., col. 9, lines 40-50. There is no "preamble consisting of a sync sequence of S bits". (Waraksa et al. provides a sync means by appending an illegal Miller line code to the Miller line codes associated with the 48-bit "code word". Waraksa et al., col. 9, lines 52-55.) There is no "preamble consisting of a sync sequence of S bits" in Waraksa et al.'s "code word".

Limitation [6]

Since Waraksa et al. does not disclose receiving a data sequence containing a "message" (Waraksa et al.'s "code word", col. 9, line 50), "the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits" (see discussion under the ***Limitation [3]*** heading), Waraksa et al. obviously does not disclose limitation [6], "a means for extracting the tag data from the received data sequence utilizing the identification of the preamble."

The examiner argues that "Waraksa uses the sync sequence as a preamble to pre-empt the data sequence, therefore it is known by Waraksa that the data sequence follows the sync sequence." 08/12/03 Office Action, p. 14. Waraksa et al.'s illegal Miller line code is not a "preamble" as defined in claim 32. Waraksa et al. do not include a "preamble" in their "code word" and consequently, Waraksa et al. do not have the means for extracting data from the received "code word" utilizing the identification of the preamble accomplished by the limitation [5] means.

> **"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."** ***Verdegaal Bros. v. UnionOil Co. of California,*** **2 USPQ2d 1051, 1053 (Fed. Cir. 1987). (Cited in MPEP § 2131.)**

Waraksa et al. does not describe each and every element of claim 32 and therefore did not anticipate applicants' claim-32 invention.

Claim 32 is written in a means-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph:

> **"As a consequence of a decision by the Court of Appeals for the Federal Circuit in its *en banc* decision *In re Donaldson Co.*, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.**

Construing Claim 32

Waraksa et al.'s digital data detector circuit 106 (Fig. 13a) detects the beginning of a message from the unique sync pattern, demodulates the PSK encoded signal, and supplies the resulting Miller encoded data to microcomputer 102. Waraksa et al., col. 11, lines 23-43.

The microcomputer 102 simply converts the Miller-encoded data into regular message bits, compares the message bits with data stored in memory, and based on the results of this comparison, controls the activation of various function. Waraksa et al., col. 11, lines 44-54.

What Waraksa et al. does not disclose is applicants' means for accomplishing Limitations [3], [4], [5], and [6]. Applicants' embodiment of the means for accomplishing the aforementioned limitations is microprocessor 17 (Fig. 1) which performs the process shown in Fig. 10 (Specification, paragraphs 0085-0088) or the process shown in Fig. 11 (Specification, paragraphs 0089-0093). Waraksa et al., because of their use of a special "sync pattern" that cannot be duplicated by a sequence of ordinary message bits, does not have to search the received data for the beginning of the tag data. Applicants must examine the received data, bit by bit, to determine the beginning of the tag data.

There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim 32 invention.

Claim 72

Claim 72 reads as follows:

72. *(currently amended) A method of receiving* ***[1] a data sequence transmitted by a tag consisting of a message repeated a plurality of times, the message comprising a preamble, a tag data group of T bits, and an error-detecting group of E bits, the preamble consisting of a sync sequence of S bits, [2] the tag data group and the error-detecting group possibly including false-sync sequences,*** *the method comprising the steps:*

[3] receiving the data sequence transmitted by the tag;

[4] detecting each sync sequence in the received data sequence;

[5] identifying the preamble;

[6] extracting the tag data group from the received data sequence utilizing the identification of the preamble.

The limitations of method claim 72 are essentially the same as those of apparatus claim 32. As discussed above under the ***Claim 32*** heading, Waraksa et al. does not disclose Limitations [1], [2], [3], [4], [5], and [6].

Waraksa et al. does not describe each and every element of claim 72 and therefore did not anticipate applicants' claim-72 invention.

Claim 72 is written in a step-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph.

Waraksa et al.'s digital data detector circuit 106 (Fig. 13a) detects the beginning of a message from the unique sync pattern, demodulates the PSK encoded signal, and supplies the resulting Miller encoded data to microcomputer 102. Waraksa et al., col. 11, lines 23-43.

The microcomputer 102 simply converts the Miller-encoded data into regular message bits, compares the message bits with data stored in memory, and based on the results of this comparison, controls the activation of various function. Waraksa et al., col. 11, lines 44-54.

What Waraksa et al. does not disclose is applicants' means for accomplishing Limitations [1], [2], [3], [4], [5], and [6]. Applicants' embodiment of the means for accomplishing the aforementioned limitations is microprocessor 17 (Fig. 1) which performs the process shown in Fig. 10 (Specification, paragraphs 0085-0088) or the process shown in Fig. 11 (Specification, paragraphs 0089-0093). Waraksa et al., because of their use of a special "sync pattern" that cannot be duplicated by a sequence of ordinary message bits, does not have to search the received data for the beginning of the tag data. Applicants must examine the received data, bit by bit, to determine the beginning of the tag data.

There is no equivalency between the operations performed by Waraksa et al.'s digital data detector circuit 106 and microcomputer 102 and applicants' microprocessor 17, and consequently, Waraksa et al. did not anticipate applicants' claim-72 invention.

IV. WHETHER CLAIMS 36-40 ARE UNPATENTABLE UNDER 35 U.S.C. § 102(E) IN VIEW OF BUCHELE (U.S. 5,276,910).

CLAIMS 36 AND 39

Claim 36 reads as follows:

36. A reader for use with a tag, the reader comprising:

a coil;

at least one capacitor;

[1] a means for coupling the capacitor(s) to the coil;

[2] a means for driving the coil through the capacitor(s) with a driving signal, *the means consisting of four field-effect transistors connected in a bridge arrangement, two opposing junctions being connected to a power supply, the driving signal being available at the remaining two opposing junctions, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor;*

a means for generating at least one control signal.

Limitation [1]

Limitation [1] of claim 36 is written in a means-plus-function format and is thus subject to the requirements of 35 U.S.C. 112, sixth paragraph:

> "As a consequence of a decision by the Court of Appeals for the Federal Circuit in its en banc decision In re Donaldson Co., 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994), "examiners must interpret a 35 U.S.C. 112, sixth paragraph 'means or step plus function' limitation in a claim as limited to the corresponding structure, materials or acts described in the specification and equivalents thereof. . . ." MPEP § 2181.

Applicants' means for coupling the capacitor(s) to the coil is shown in Fig. 1 as coupling circuit 7. Embodiments of coupling circuit 7 are shown in Figs. 2, 3, 4, and 5 and described in paragraphs 45, 46, and 47. In the direct connection of Fig. 2, one capacitor terminal connects to a terminal of coil 5 and the other capacitor terminal connects to a terminal of driver 11 (see Fig. 1). In the transformer coupling circuits of Figs. 3, 4, and 5, one capacitor terminal connects to a terminal of the primary winding and the other capacitor terminal connects to a terminal of driver 11 (see Fig. 1). The terminals of the secondary winding connect to coil 5.

In Buchele, the examiner identifies capacitor 160 as being coupled to coil 190 (Fig. 2). 08/12/03 Office Action, p. 5. However, capacitor 160 is not coupled to coil 190 either directly or by a transformer or an equivalent thereof. The connection of capacitor 160 across the source 170 of DC power for driver 110 does not constitute the coupling of capacitor 160 to coil 190.

Buchele does not disclose either the direct coupling or coupling through a transformer of capacitor 160 to coil 190 and consequently, did not anticipate limitation [1].

Limitation [2]

The Buchele's "H-bridge output driver 110" (Buchele, col. 5, lines 61-68) is the structural equivalent of the "bridge arrangement" specified in limitation [2]. Buchele's opposing junctions 146,156 and 124,134 are connected to a power supply (battery 170) just as limitation [2] specifies. Buchele's remaining two opposing junctions 136,144 and 126,154 are the source of the driving signal for coil 190 ("high power PWM signal", Buchele, col. 5, lines 46-52) just as limitation [2] specifies. The current flow through Buchele's H-bridge transistors are controlled by a control signal applied to the gate of each transistor (Buchele, col. 6, lines 21-40), just as limitation [2] specifies.

What Buchele does not disclose is the "high power PWM signal" (that exists at opposing junctions 136,144 and 126,154) feeding through capacitor(s) to coil 190. There are no capacitors in the lines connecting opposing junctions 136,144 and 126,154 to coil terminals 192 and 194. Thus, Buchele also does not disclose limitation [2].

Since Buchele does not disclose one or more limitations of claim 36, Buhele did not anticipate claim 36.

Buchele did not anticipate claim 39 because of its dependency on claim 36.

CLAIM 37

All of the transistors shown in Buchele's H bridge (Fig. 2) are n-channel devices. Buchele does not disclose the claim-37 limitation "wherein the bridge circuit comprises two series-connected P- and N-channel field effect transistors connected in parallel, the junction of the P devices and the junction of the N devices being connected to a voltage supply, the driving signal being available at the junctions of the P and N devices."

Since Buchele does not disclose one or more limitations of claim 37, Buchele did not anticipate claim 37.

CLAIM 38

Buchele does not disclose in his H bridge (Fig. 2) "a diode connected between gate and source of each transistor to protect the gates from voltage spikes" and "a resistor in series with each gate of each transistor to suppress ringing in the gate circuit when the transistor is turned on."

Since Buchele does not disclose one or more limitations of claim 38, Buchele did not anticipate claim 38.

CLAIM 40

Buchele does not disclose in his H bridge (Fig. 2) "a two-winding transformer associated with each transistor, a control signal being fed into one winding of a transformer, the other winding being connected between gate and source electrodes of the associated transistor.

Since Buchele does not disclose one or more limitations of claim 40, Buchele did not anticipate claim 40.

V. WHETHER CLAIMS 70,71, 73-80 ARE UNPATENTABLE UNDER 35 U.S.C. § 102(E) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194.

CLAIM 70

Claim 70 reads as follows:

70. A method for interrogating a tag comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to a tag in the alternating magnetic field.

Carroll et al. does not disclose the limitation in boldface.

Carroll et al. discloses controller 10 and transponder 40 which communicate with one another by performing the following steps:

- Controller 10 initiates communications by transmitting an unmodulated carrier (col. 9, lines 4-6);
- Transponder 40 receives the unmodulated carrier from controller 10, transmits a carrier obtained by dividing the frequency of the received unmodulated carrier by two (col. 13, lines 28-42), embeds a bit timing clock signal in the transmitted carrier (col. 14, lines 60-66; col. 20, lines 33-43)*, the embedded bit timing clock signal being obtained by further dividing down the frequency of the received unmodulated carrier to the bit rate (col. 12, lines 26-34), and embeds a data bit sequence in the transmitted carrier following the transmission of the embedded bit timing clock signal (col. 14, line 66 - col. 15, line 13);

- Controller 10 extracts the bit timing signal from the carrier received from transponder 40 (col. 15, lines 54-63), transmits data to transponder 40 in accordance with the bit timing signal received from transponder 40 (col. 16, lines 1-10, 46-52);**
- Transponder 40 extracts data from the carrier received from controller 10 using its own bit timing signal. Since controller 10's data was transmitted utilizing the bit timing clock signal supplied by transponder 40, there was no need for controller 10 to include a bit timing clock signal in its transmission to transponder 40.

* *Line coding is the process of converting or coding sequentially transmitted abstract symbols (such as "0" and "1") into real, temporal waveforms. Manchester line coding converts a "0" into a square wave that is negative during the first half of a bit period and positive during the second half. The Communications Handbook, Editor-in-Chief Jerry D. Gibson, CRC Press, Inc. Boca Raton, FL (1987) p. 386-394. A sequence of 4 "0's" results in a square wave having a frequency equal to the bit rate.*

** *The synchronization logic bits D0-D3 transmitted by controller 10 are a repetition of synchronization logic bits D0-D3 transmitted by transponder 40. Controller 10's synchronization bits do not result in the embedding of a bit-timing clock signal in controller 10's carrier because the controller 10 does not use Manchester line coding in transmitting data. To transmit a "0", controller 10 transmits a carrier having a frequency of 125 kHz for the entire bit period. To transmit a "1", controller 10 transmits a carrier having a frequency that shifts from 125 kHz to 116.3 kHz and back during a bit period (col. 16, lines 52-55). The transmission of the synchronization block consisting of 4 "0's" results in the transmission of a carrier having a frequency of 125 kHz for the entire 4-bit period.*

Thus, Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field."

The examiner argues that the synchronization block consisting of 4 "0's" which is transmitted by controller 10 constitutes a bit-timing clock signal. 08/12/03 Office Action, p. 16. As we point out above, there is no bit timing information in the transmission of 4 "0's" by controller 10. Confirmation of this assertion is provided by the fact that Carroll et al. does not disclose transponder

40 extracting a bit-timing clock signal from the signal received from controller 10. Carroll et al. only discloses a divide-by-64 timing control 60 which is simply a synchronous counter driven by the carrier received from controller 10 (col. 17, lines 39-51).

Carroll et al. does disclose the extraction of a bit-timing clock signal by controller 10 (see Fig. 2E). Why would controller 10 need to extract the bit-timing clock signal from transponder 40's carrier if controller 10 had supplied the bit-timing clock signal to transponder 40 in the first place?

Since Carroll et al. does not disclose at least one limitation of claim 70, Carroll et al. did not anticipate claim 70.

CLAIM 71

Claim 71 reads as follows:

71. A method for interrogating a tag, ***[1] the tag responding to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator,*** *the method comprising the steps:*

[2] generating a bit-timing clock signal;

[3] generating an alternating magnetic field in which the bit-timing clock signal is embedded;

[4] extracting data transmitted by the tag utilizing the bit-timing clock signal.

Carroll et al. does not disclose any of the four limitations shown in boldface.

Limitation [1]

Carroll et al.'s transponder 40 responds to an interrogation by transmitting a sequence of bits in accordance with a bit-timing clock signal generated by transponder 40, but the bit-timing clock signal is NOT synchronized with a bit-timing clock signal originating from controller 10 since controller 10 does NOT transmit a bit-timing clock signal to transponder 40.

Carroll et al.'s bit-timing clock in transponder 40 is obtained by dividing down the frequency of the interrogating signal. Carroll et al., col. 12, line 20 - col. 13, line 7. As discussed above under the ***Claim 70*** heading, controller 10 does not transmit a bit-timing clock signal to transponder 40, and transponder 40 does not require one.

The examiner argues that limitation [1] appears in the preamble of the claim and merely recites the purpose of a process. 08/12/03 Office Action, p. 16. However, *The Manual of Patent Examining Procedure* emphasizes:

> **"Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation. See, e.g. *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989)."** MPEP § 2111.02.

In the case of a method claim, it would be appropriate to substitute "steps" for "structure". For example, "a method for getting from one place to another" is merely a statement of the purpose of the method and does not imply any limitations on the method steps. On the other hand, "a method for communicating using the Verizon Wireless network" is not merely a statement of use but also implies certain limitations on the method steps if the method steps are to be compatible with the Verizon Wireless network.

In the present case of a method for interrogating a tag which responds "to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator", the "for use" clause, like the cell phone example, is not merely a statement of use but also implies limitations on the method steps if the method steps are to be compatible with tags having the specified characteristics. Consider, for example, the consequences of omitting "and synchronized with a bit-timing clock signal originating with the interrogator." Such an omission would have a profound effect on the scope of limitation [4] since extracting data transmitted by the tag would be significantly more complicated if the bit-timing clock signals of interrogator and tag were not synchronized.

This example demonstrates that limitation [1] affects the scope of at least one of the other limitations and must be taken into account in determining the patentability of the claim.

One might ask whether a method for interrogating a tag which responds "to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator" asserts step limitations that are not already fully and intrinsically set forth by the limitations in the body of the claim:

> **"If the body of a claim fully and intrinsically sets forth all of the limitations of the claimed invention, and the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction.** ***Pitney Bowes, Inc. v. Hewlett-Packagd Co.*****, 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999)."** MPEP § 2111.02.

None of the body elements of the claims at issue disclose either separately or in combination limitation [1] and thus, this limitation represents an additional limitation which must be treated as a legitimate claim limitation and not merely "a statement of purpose or use."

Limitation [2]

Carroll et al.'s controller 10 does not generate a bit-timing clock signal which, as the claim preamble specifies, is the bit-timing reference for both controller 10 and transponder 40. Carroll et al.'s transponder 40 generates a bit-timing clock signal and transmits it to controller 10 as sync block 102 in configuration word 100 (Fig. 4A). Sync block 102 consists of four "0's" which, after being converted to Manchester line codes, become a square wave having a frequency equal to the bit rate. This square wave is used by controller 10 as the bit-timing clock signal in extracting the other parts 106, 108, and 110 of configuration word 100 from the carrier transmitted by transponder 40.

Controller 10 transmits command word 112 in bit for bit synchronization with configuration word 100 including sync block 114 consisting of four "0's" (Fig. 4B, col. 16, lines 1-10). Controller 10 does not use Manchester line codes, however, and the four "0's" are not converted to the square-wave bit-timing clock signal as was the case with transponder 40's transmission. Instead, each "0" becomes a carrier lasting for the bit period with a frequency of 125 kHz. (A "1" is transmitted by toggling the carrier frequency between 125 kHz and 116.3 kHz (col. 11, lines 11-26).) Four "0's" becomes a carrier lasting for four bit periods with a frequency of 125 kHz.

Thus, there is no bit-timing information available in controller 10's transmission of four "0's". Controller 10 neither generates a bit-timing clock signal nor does it transmit the bit-timing clock signal it receives from transponder 40 back to transponder 40.

The examiner argues that "[t]he sync signal that is generated in element 70 of Carroll is a bit timing clock signal." 08/12/03 Office Action, p.17. The sync signal referred to by the examiner has to do with acts performed in transponder 40. Limitation [2] refers to an act performed by the "interrogator", the counterpart in Carroll et al. being controller 10. Controller 10 does not generate a bit-timing clock signal.

Limitation [3]

Carroll et al.'s controller 10 does not embed a bit-timing clock signal in the interrogating signal transmitted to transponder 40. Please see discussion above under the **CLAIM 70** heading.

The examiner argues that "[t]he sync signal that is generated in element 70 of Carroll is a bit timing clock signal and is transmitted through the PSK modulator." 08/12/03 Office Action, p. 17. The sync signal referred to by the examiner has to do with acts performed in transponder 40. Limitation [3] refers to an act performed by the "interrogator", the counterpart in Carroll et al. being controller 10. Controller 10 does not generate an alternating magnetic field in which the bit-timing clock signal is embedded.

Limitation [4]

Carroll et al.'s controller 10 does not extract the data carried by the signal transmitted by transponder 40 using a bit-timing signal originating in controller 10. Carroll et al.'s controller 10 does not generate such a signal (see discussion above under ***Limitation [2]*** heading) and obviously cannot use it in extracting the data sent by transponder 40.

Carroll et al. does not describe each and every element of claim 71 and therefore did not anticipate applicants' claim-71 invention.

CLAIM 73

Claim 73 reads as follows:

73. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

driving the resonating circuit with a driving signal;

maintaining the resonating circuit in resonance;

embedding the sequence of bits to be communicated to the reader in the driving signal.

Carroll et al. does not disclose the limitation shown in boldface. Carroll et al. discloses the use of a resonating circuit which is tuned to the frequency of the interrogating signal. Carroll et al., col. 12, lines 1-19. Nothing is said about maintaining the resonating circuit in resonance.

The examiner argues that maintaining the resonating circuit in resonance "is inherent to any receiver that is attempting to receive data on a carrier (which Carroll does)." 08/12/03 Office Action, p. 17. The examiner is incorrect. Maintaining the resonating circuit in resonance is NOT inherent to any receiver that is attempting to receive data on a carrier. The examiner was obligated to supply evidence of inherency and did not do so:

> **"To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so**

recognized by persons of ordinary skill." *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d, 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

Carroll et al. does not describe each and every element of claim 73 and therefore did not anticipate applicants' claim-73 invention.

CLAIM 74

Claim 74 reads as follows:

*74. A method for responding to the establishment of an alternating magnetic field by a reader, **[1] the reader embedding a bit-timing clock signal in the alternating magnetic field** and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:*

deriving a signal from the alternating magnetic field;

[2] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field;

[3] performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

[4] identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

Carroll et al. does not disclose any of the limitations shown in boldface.

Limitation [1]

This limitation is the same as the boldface limitation of claim 70. Please see the argument presented above under the **CLAIM 70** heading in support of the assertion that Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field".

The examiner states that this limitation, since it appears in the preamble of the claim, was not "given patentable weight." 08/12/03 Office Action, p. 17. However:

> **"If the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim."** ***Pitney Bowes, Inc. v. Hewlett-Packard Co.*****, 182 F.3d 1298, 1305, 51 USPQ2D 1161, 1165-66 (Fed. Cir. 1999).**

Certainly, the preamble in the present case is necessary to give meaning to the claim and should be construed as if in the balance of the claim.

Limitation [2]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". There is no bit-timing clock signal available to Carroll et al.'s transponder 40 (see discussion under the **CLAIM 70** heading), and consequently, there is no way for transponder 40 to generate a bit-timing clock signal that is synchronized to an embedded bit-timing clock signal.

Note that the only clock signal available to Carroll et al.'s "divide-by-64" timing control 60 (Fig. 3), which supplies all the timing signals for transponder 40, is the incoming FSK modulated data signal. Carroll et al., col. 12, lines 20-25. The "divide-by-64" timing control 60 is nothing more

than a digital counter. Carroll et al., col. 12, lines 26-34. Nothing is said about generating a bit-timing clock signal and synchronizing it to an embedded bit-timing signal.

The examiner states that "applicant argues (2) that the bit timing clock signal is not synchronized to the bit timing clock signal from the interrogator." 08/12/03 Office Action, p. 18. This is not a correct statement of applicants' argument. Applicants argue that there is no bit-timing clock signal available from controller 10, and consequently, it would be impossible for transponder 40 to synchronize its locally-generated bit-timing clock signal with a non-existent bit-timing clock signal from controller 10.

The examiner argues that "[t]he sync generator 70 is synchronized to the received clock signal since the timing control element 60 drives all the elements that follow, etc 64,48,68 and 70." 08/12/03 Office Action, p. 18. The "received clock signal" that the examiner refers to is presumably the FSK modulated signal of frequency 125 kHz from controller 10. col. 7, lines 22-25; col. 17, lines 39-52. This is the carrier of the data that controller 10 transmits to transponder 40. It is not a bit-timing clock signal to which the bit-timing clock signal generated by transponder 40 is synchronized.

As we have emphasized repeatedly, controller 10 does NOT provide a bit-timing clock signal to which transponder 40's locally-generated bit-timing clock signal could be synchronized.

Carroll et al. does not disclose limitation [2].

Limitation [3]

There is nothing in Carroll et al. that is even suggestive of Limitation [3].

The examiner states that "applicant argues (3) that Carroll does not use weighted integration to identify the bit period." 08/12/03 Office Action, p. 18. Applicants do not make this argument.

Applicants argue that Carroll et al. do not disclose limitation [3] which specifies "performing at least one weighted integration of the derived signal over a bit period USING THE BIT-TIMING CLOCK SIGNAL TO IDENTIFY THE BEGINNING AND END OF A BIT PERIOD."

The examiner argues that [d]ividing by 64 is weighted integration for providing the claimed feature. The divide-by-64 timing control 60 is simply a synchronous counter (col. 18, lines 58-60). It has nothing to do with performing a weighted integration of a received signal. A weighted integration results from the multiplication of the signal received during a bit period by a weighting function and integrating the result.

Carroll et al. does not disclose limitation [3].

Limitation [4]

Carroll et al. does not disclose "weighted integrations" and obviously does not disclose the use of weighted integrations in identifying the bit being transmitted.

The examiner argues that "[e]lement 62 does use the weighted integration to identify the incoming data." 08/12/03 Office Action, p. 18. Element 62 is an "address register" used to access the selected bits within the words of the non-volatile memory array (col. 18, lines 14-17). This "address register" has nothing to do with identifying the bit being transmitted during each bit period. FSK detector 64 identifies the bit being transmitted simply by measuring the frequency of the FSK modulated signal output from controller 10 (col. 18, lines 44-57). No weighted integrations are involved.

Carroll et al. does not disclose limitation [4].

Carroll et al. does not describe each and every element of claim 74 and therefore did not anticipate applicants' claim-74 invention.

CLAIM 75

Claim 75 reads as follows:

*75. A method for responding to the establishment of an alternating magnetic field by a reader, **[1] a bit-timing signal being embedded in the alternating magnetic field by the reader**, the method comprising the steps:*

deriving a signal from the alternating magnetic field;

[2] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field;

generating an alternating magnetic field;

[3] modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal.

Carroll et al. does not disclose any of the limitations shown in boldface.

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field". Please see the discussion under the **CLAIM 74, *Limitation [1]*** heading including responses to the examiner's arguments.

Limitation [2]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field". Please see the discussion under the **CLAIM 74, *Limitation [2]*** heading including responses to the examiner's arguments.

Limitation [3]

Carroll et al. does not disclose the transmission of bits by Carroll et al.'s transponder 40 to controller 10 wherein the start of each transmitted bit is governed by a bit-timing clock signal that originates in controller 10. A bit-timing clock signal which is synchronized with a bit-timing clock signal that originates in controller 10 is simply not available in transponder 40 (see ***Limitations [1] and [2]***).

Carroll et al. does not describe each and every element of claim 75 and therefore did not anticipate applicants' claim-75 invention.

CLAIM 76

Claim 76 reads as follows:

76. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

[1] embedding a bit-timing clock signal in the alternating magnetic field;

extracting data communicated by the responder from an alternating magnetic field generated by the responder;

the method performed by the responder comprising the steps:

[2] extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator;

[3] generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator;

generating an alternating magnetic field;

[4] embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder.

Carroll et al. does not disclose any of Limitations [1], [2], [3], and [4].

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field", a limitation also present in claim 70. For arguments in support of this assertion, please see the discussion above under the ***Claim 70*** heading.

Limitation [2]

Since Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field", it follows that Carroll et al. could not and does not disclose "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator". The only extraction performed by Carroll et al.'s transponder 40 is the extraction of data from the incoming FSK modulated signal from controller 10 (col. 12, lines 20-34), the FSK modulated signal being produced by shifting the frequency of the signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a data pulse. Carroll et al., col. 7, lines 16-29.

Extracting the data from an FSK modulated signal is NOT the same as extracting a bit-timing clock signal.

The examiner argues that "[e]lements 58 and 60 extract the bit timing clock signal from the carrier generated by the interrogator." 08/12/03 Office Action, p. 19. Element 58 amplifies the 125-kHz carrier transmitted by controller 10, and element 60 divides the 125-kHz carrier by 64 to obtain a clock signal having a frequency equal to the bit rate (Fig. 3, divide-by-64 timing control 60). But generating a clock signal having the a frequency equal to the bit rate by dividing down the frequency of the carrier signal is not the same as "EXTRACTING a bit-timing clock signal that is embedded in the carrier signal. The dictionary definition of "extract" is "to pull or draw out". *The Random House College Dictionary, Revised Edition*, Random House, Inc. 1988. "Pulling or drawing out the bit-timing clock signal from the alternating magnetic field generated by the interrogator" implies that there is a unique bit-timing clock signal contained in the alternating magnetic field which can be pulled out. The clock signal that one obtains by dividing down the carrier signal is not unique. There are 64 possible clock signals that could be obtained, depending on when the divide-by-64

timing control begins to count. There is no reasonable interpretation of the language of limitation [2] that would allow one to conclude that a synchronous counter is a disclosure of the limitation.

Limitation [3]

Carroll et al. does not disclose "generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator".

Carroll et al. discloses the generation of a clock signal having a frequency equal to the bit rate (see ***Limitation [2]***). However, Carroll et al. does not disclose any operations that suggest synchronizing this clock signal with any other clock signal having a frequency equal to the bit rate let alone a clock signal having a frequency equal to the bit rate and originating with controller 10.

The examiner argues that "[t]he sync generator 70 is synchronized to the received clock signal since the timing control element 60 drives all the elements that follow, etc 64,48,68 and 70." 08/12/03 Office Action, p. 19. The "received clock signal" which the examiner refers to is the carrier transmitted by controller 10. It is not the bit-timing clock signal embedded in the carrier that is specified in Limitation [3].

Limitation [4]

Carroll et al. does not disclose the transmission of bits by transponder 40 to controller 10 wherein the start of each transmitted bit is governed by a bit-timing clock signal that originates in controller 10. Please see the discussion under the ***Claim 75, Limitation [3]*** headings.

Carroll et al. does not describe each and every element of claim 76 and therefore did not anticipate applicants' claim-76 invention.

CLAIM 77

Claim 77 reads as follows:

77. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

[1] embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to the responder in the alternating magnetic field; the method performed by the responder comprising the steps:

[2] extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator;

[3] performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

[4] identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

Carroll et al. does not disclose any of Limitations [1], [2], [3], and [4].

Limitation [1]

Carroll et al. does not disclose "embedding a bit-timing clock signal in the alternating magnetic field", a limitation also present in claim 70. For arguments in support of this assertion, please see the discussion above under the **CLAIM 70** heading.

Limitation [2]

Carroll et al. does not disclose "extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator", a limitation also present in claim 76. For arguments in support of this assertion, please see the discussion above under the **CLAIM 76, *Limitation [2]*** headings.

Limitation [3]

Carroll et al. does not disclose "performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period", a limitation also present in claim 74. For arguments in support of this assertion, please see the discussion above under the **CLAIM 74, *Limitation [3]*** heading.

Limitation [4]

Carroll et al. does not disclose "identifying the bit being transmitted during each bit period utilizing the weighted integration(s)", a limitation also present in claim 74. For arguments in support of this assertion, please see the discussion above under the **CLAIM 74, *Limitation [4]*** heading.

Carroll et al. does not describe each and every element of claim 77 and therefore did not anticipate applicants' claim-77 invention.

CLAIM 78

Claim 78 reads as follows:

78. An apparatus for practicing the method of claim 73.

Carroll et al. did not anticipate claim 73 and consequently did not anticipate claim 78 which depends from claim 73.

CLAIM 79

Claim 79 reads as follows:

79. An apparatus for practicing the method of claim 76.

Carroll et al. did not anticipate claim 76 and consequently did not anticipate claim 79 which depends from claim 76.

CLAIM 80

Claim 80 reads as follows:

80. An apparatus for practicing the method of claim 77.

Carroll et al. did not anticipate claim 77 and consequently did not anticipate claim 80 which depends from claim 77.

VI. WHETHER CLAIMS 1, 3, 41, AND 43 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CHATELOT (U.S. 4,864,633) AND KURUSU (U.S. 3,587,017).

CLAIM 1

Claim 1 reads as follows:

1. (currently amended) A reader for use with a tag that communicates data to the reader, the reader comprising:

[1] a transformer having a plurality of windings, each winding having first and second terminals;

a coil driver having first and second output terminals;

[2] two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer;

[3] a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer;

[4] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer.

Neither Chatelot nor Kurusu disclose the limitations in boldface.

To establish a *prima facie* case of obviousness, three basic criteria must be satisfied:

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP § 2142.

Limitation [1]

Chatelot does not disclose the use of a transformer by a reader in communicating with a tag. Kurusu discloses a transformer as an impedance matching device between a filter and an amplifier in an overvoltage-protecting arrangement. Kurusu's application does not envision the use of a single transformer in both transmitting and receiving signals as specified by Limitations [2], [3], and [4].

Thus, neither Chatelot nor Kurusu disclose a multi-purpose transformer as specified in claim 1.

Limitation [2]

As the examiner has pointed out, Chatelot does not disclose Limitation [2]. 08/12/03 Office Action, p. 6.

Kurusu shows a receiving antenna 11 that feeds a received signal through a filter 13 to amplifier 12 which outputs an amplified version of the received signal. Amplifier 12 includes input coupling transformer 17, capacitor 22 connected across the input winding of transformer 17, and RC circuit 21 which (together with RC circuit 23) provides proper biasing of transistor 16. Kurusu, Fig. 1.

The examiner argues that Chatelot's capacitors 19 are analogous to Kurusu's capacitor in RC circuit 21 and Chatelot's transmission coil 13 is analogous to Kurusu's receiving antenna 11. *See*

Chatelot, Fig. 3. The examiner then concludes that it would be obvious to one skilled in the art to combine Kurusu's transformer 17 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention.

With respect to teaching or suggesting limitation [2], there is no teaching of "two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding of the transformer". The capacitor in RC circuit 21 (Kurusu, Fig. 1) is connected to ground rather than being analogous to Chatelot's capacitors 19 which provide passageways for driving signals to coil 13. Thus, Kurusu provides no information as to how to incorporate Kurusu's transformer in Chatelot's invention. Does the person skilled in the art simply insert Kurusu's transformer 17 between Chatelot's capacitors 19 and coil 13 as applicants specify in claim 1? Or does the person skilled in the art place Kurusu's transformer 17 on the other side of Chatelot's capacitors 19? There is no teaching as to what to do.

Limitation [3]

Chatelot does not disclose the use of a transformer in communicating with data carrier 12. Chatelot, Figs. 2 and 3.

Kurusu discloses the two terminals of antenna 11 connected to the two input terminals of filter 13. Neither Chatelot nor Kurusu disclose "a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer."

Limitation [4]

Limitation [4] specifies "a data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer."

Chatelot does not disclose this limitation since Chatelot does not disclose a transformer located between capacitor(s) 19 and coil 13. Chatelot extracts data from signals picked up from the capacitor terminals NOT connected to the coil (Chatelot, Fig. 3), and consequently, even if Chatelot had disclosed a transformer located between capacitor(s) 19 and coil 13, he would not have disclosed limitation [4].

Kurusu discloses an amplifier connected to a winding of transformer 17, but transformer 17 is not the multiple-purpose transformer called for by Limitations [2], [3], and [4].

There is no teaching in Chatelot and/or Kurusu that would cause a person skilled in the art to incorporate the transformer disclosed by Kurusu in Chatelot's invention at a location between capacitor(s) 19 and coil 13.

With respect to motivation, there is nothing in Chatelot that suggests the substitution of a transformer for the direct connections of capacitors 19 to coil 13. There is nothing in the category of "knowledge generally available to one of ordinary skill in the art" that suggests this substitution.

Nor would a person skilled in the art be motivated to substitute a transformer employed in an overvoltage protecting arrangement for an RF amplifier used to amplify received signals. Kurusu, col. 1, lines 5-73. The use of a transformer for coupling received signals into an amplifier (Kurusu) has little or nothing to do with coupling a driving signal to a coil (Chatelot).

The examiner responds to these arguments by arguing that the general knowledge that a transformer coupling provides isolation between circuits is sufficient motivation. 08/12/03 Office

Action, p. 21. The examiner did not explain why isolation between circuits is needed or even desirable in the Chatelot invention.

Chatelot and Kurusu in combination fail to teach all of the claim limitations of claim 1. Even if the combination did teach all of the claim limitations of claim 1, there is no motivation for a person skilled in the art to make such a combination. The examiner did not establish the *prima facie* obviousness of claim 1.

CLAIM 3

Claim 3 reads as follows:

3. (currently amended) The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the second winding.

Neither Chatelot nor Kurusu show the configuration specified in claim 3. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-3 limitations. For details, please see discussion above under the **CLAIM 1** heading.

The examiner has not established the *prima facie* obviousness of claim 3.

CLAIM 41

Claim 41 reads as follows:

41. A tag for use with a reader, the tag comprising:

[1] a transformer having a plurality of windings, each winding having first and second

terminals;

[2] a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[3] a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[4] a coil driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

[5] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer;

[6] a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer.

Limitation [1]

Chatelot does not disclose the use of a transformer by either a reader or a tag in communicating.

Kurusu discloses a transformer as an impedance matching device between a filter and an amplifier in an overvoltage-protecting arrangement. Kurusu's application does not envision the use of a single transformer in both transmitting and receiving signals and in power extraction as specified by Limitations [2], [3], [4], [5], and [6].

Thus, neither Chatelot nor Kurusu disclose a multi-purpose transformer as specified in claim 41.

Limitation [2]

The two terminals of Kurusu's antenna 11 (corresponding to applicants' coil) connects to the two terminals of filter 13. Thus, neither Chatelot nor Kurusu discloses "a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Limitation [3]

Only one terminal of Kurusu's capacitor 19 connects to antenna winding 19. Thus, neither Chatelot nor Kurusu disclose "a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

The first terminals of Chatelot's capacitors 19 connect to the first and second terminals of Chatelot's transmission circuit 21 (applicants' driver). The second terminals of Chatelot's capacitors 19 connect to the first and second terminals of Chatelot's coil 13.

The examiner argues that Chatelot's capacitors 19 are analogous to Kurusu's capacitor in RC circuit 21 and Chatelot's transmission coil 13 is analogous to Kurusu's receiving antenna 11. *See* Chatelot, Fig. 3. The examiner then concludes that it would be obvious to one skilled in the art to combine Kurusu's transformer 17 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention. Since the first terminal of Kurusu's capacitor in RC circuit 21 is connected to a first terminal of winding 18 of transformer 17 and the second terminal of

Kurusu's capacitor is connected to a first terminal of winding 19 of transformer 17, this arrangement with Chatelot's capacitors 19 taking the place of Kurusu's capacitor does not result in the arrangement specified by the limitation "a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Limitation [4]

One terminal of Chatelot's transmission circuit 21 ("driver") connects to one terminal of Chatelot's capacitor 19 and according to the examiner's suggested connection arrangement would connect to the same terminal of the winding 19 that the capacitor is connected to. Kurusu does not disclose a driver and provides no insight as to how a driver would be incorporated in his invention.

The examiner has not suggested how the other terminal of Chatelot's transmission circuit should be connected to a transformer winding.

There is no basis for arguing that Chatelot and Kurusu can be combined in a way that will result in the limitation "a driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Limitation [5]

One terminal of Chatelot's reception circuit 22 ("data extractor") connects to one terminal of Chatelot's capacitor 19 and according to the examiner's suggested connection arrangement would connect to the same terminal of winding 19 that the capacitor is connected to. The input terminals to Kurusu's transistor 16 (corresponding to the input of a "data extractor") would be connected, according to the examiner's suggested arrangement, to the same terminal of winding 18 that the

capacitor is connected to and to the terminal of winding 19 that the capacitor is not connected to. This connection arrangement is not the one specified in the limitation "a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer."

Limitation [6]

And finally, neither Chatelot nor Kurusu disclose circuitry, either separately or in combination, which would correspond to the limitation "a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Neither Chatelot nor Kurusu disclose the limitations specified in claim 41. Neither Chatelot nor Kurusu provide motivation to a person skilled in the art to attempt a combination of Chatelot and Kurusu that would result in applicants' claim-41 invention.

The examiner has not established the *prima facie* obviousness of claim 41.

CLAIM 43

Claim 43 reads as follows:

43. The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor and the driver being connected to the first winding, the coil, the data extractor, and the power extractor being connected to the second winding.

Neither Chatelot nor Kurusu disclose "the capacitor and the driver being connected to the first winding" nor do they disclose "the coil, the data extractor, and the power extractor being connected to the second winding." The references also do not provide any motivation to a person skilled in the art to incorporate a transformer in Chatelot's invention for the purpose of achieving an invention with the limitations of claim 43.

The examiner did not address the specific limitations of claim 43 in either of his office actions and has not established the *prima facie* obviousness of claim 43.

VII. WHETHER CLAIMS 1, 2, 4, 41, 42, 44, AND 45 ARE UNPATENTABLE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CHATELOT (U.S. 4,864,633) AND OGITA ET AL. (U.S. 4,278,980).

CLAIM 1

Claim 1 reads as follows:

Claim 1 reads as follows:

1. (currently amended) A reader for use with a tag that communicates data to the reader, the reader comprising:

[1] a transformer having a plurality of windings, each winding having first and second terminals;

a coil driver having first and second output terminals;

[2] two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors, the second terminals of the capacitors being connected to the first and second terminals of a winding

of the transformer;

[3] a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer;

[4] a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer.

Neither Chatelot nor Ogita et al. nor the references in combination disclose either of the limitations in boldface.

Limitation [1]

Chatelot does not disclose the use of a transformer by a reader in communicating with a tag or by a tag in communicating with a reader. Ogita et al. discloses a transformer as an impedance matching device between a coil and an amplifier. Ogita et al., Fig. 8. Ogita et al.'s application does not envision the use of a single transformer in both transmitting and receiving signals as specified by Limitations [2], [3], and [4].

Thus, neither Chatelot nor Ogita et al. disclose a multi-purpose transformer as specified in claim 1.

Limitation [2]

Chatelot discloses a transmission circuit 21 driving coil 13 through capacitors 19 connected directly to coil 13. Chatelot, Figs. 2 and 3. Thus, Chatelot discloses the first part of Limitation [2],

"two capacitors, each capacitor having first and second terminals, the first and second output terminals of the coil driver being connected to the first terminals of the capacitors."

Ogita et al. shows a receiving antenna 21 that feeds a received signal through impedance-matching transformer 31 to amplifier 37. Ogita et al., Fig. 8. Ogita et al.'s capacitor 34 is merely a tuning capacitor (Ogita et al., col. 6, lines 7-11) and not the analog of Chatelot's capacitors 19.

Ojita et al.'s teaching of the use of a tranformer for matching impedances in a receiving circuit is not a teaching of the use of a transformer in Chatelot's transmission circuit for coupling capacitors 19 to coil 13 so that transmission circuit 21 can send driving signals through capacitors 19 to coil 13.

Limitation [3]

Chatelot does not disclose the use of a transformer in communicating with data carrier 12. Chatelot, Figs. 2 and 3.

Ogita et al. discloses the two terminals of loop antenna 21 connected to an end terminal and a tap terminal (NOT the two end terminals) of winding 32 of transformer 31. Neither Chatelot nor Ogita et al. disclose "a coil having first and second terminals connected respectively to the first and second end terminals of a winding of the transformer."

Limitation [4]

Limitation [4] specifies "a data extractor having first and second terminals connected respectively to first and second terminals of a winding of the transformer."

Chatelot does not disclose this limitation since Chatelot does not disclose a transformer located between capacitor(s) 19 and coil 13. Chatelot extracts data from signals picked up from the capacitor terminals NOT connected to the coil (Chatelot, Fig. 3), and consequently, even if Chatelot had disclosed a transformer located between capacitor(s) 19 and coil 13, he would not have disclosed limitation [4].

Ogita et al. shows a receiving antenna 21 that feeds a received signal through impedance-matching transformer 31 to amplifier 37. Ogita et al., Fig. 8. Ogita et al.'s capacitor 34 is merely a tuning capacitor (Ogita et al., col. 6, lines 7-11) and not the analog of Chatelot's capacitors 19.

Ogita et al. discloses amplifier 37 connected to winding 33 of transformer 31, but transformer 31 is not the multiple-purpose transformer called for by Limitations [2], [3], and [4].

There is no teaching in Chatelot and/or Ogita et al. that would motivate a person skilled in the art to incorporate the transformer disclosed by Ogita et al. in Chatelot's invention at a location between capacitor(s) 19 and coil 13.

The examiner concludes that it would be obvious to one skilled in the art to combine Ogita et al.'s transformer 31 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-1 invention. 08/14/03 Office Action, p. 7. The problem with the examiner's conclusion is that it is not clear how this combination would be accomplished.

Capacitor 34 (Ogita et al., Fig. 8) is connected to ground rather than being analogous to Chatelot's capacitors 19 which provide passageways for driving signals to coil 13. Thus, Ogita et al. provides no information as to how to incorporate Ogita et al.'s transformer in Chatelot's invention. Does the person skilled in the art simply insert Ogita et al.'s transformer 31 between Chatelot's

capacitors 19 and coil 13 as applicants specify in claim 1? Or does the person skilled in the art place Ogita et al.'s transformer 31 on the other side of Chatelot's capacitors 19? There is no teaching in either of the references as to what to do.

With respect to motivation, there is nothing in Chatelot that suggests the substitution of a transformer for the direct connections of capacitors 19 to coil 13. There is nothing in the category of "knowledge generally available to one of ordinary skill in the art" that suggests this substitution.

Nor would a person skilled in the art be motivated to substitute a transformer employed in impedance-matching a receiving antenna to an amplifier for Chatelot's direct connections of capacitors 19 to coil 13. The use of a transformer for impedance matching in a receiving circuit (Ogita et al.) has little or nothing to do with coupling a driving signal to a coil for the purpose of interrogating a tag (Chatelot).

Nor would a person skilled in the art be motivated to use Ogita et al.'s transformer for coupling the data extractor to the coil as specified in Limitation [4]. Ogita et al. discloses nothing concerning the use of a common capacitor-coil configuration, where the coil and capacitor(s) are coupled together by a transformer means, for both transmitting and receiving signals.

The examiner argues that the motivation for incorporating Ogita et al.'s transformer in Chatelot's invention is "to provide isolation between the communication antenna coil and the other circuits in the reader." 08/12/03 Office Action, p. 7. However, such a modification would appear to be unnecessary since Chatelot states that with his reading-writing station "a rapid and reliable data exchange may be made with a user system such as a programmable automation or other system controlling an industrial process." Chatelot, col. 2, lines 3-6. Where is the motivation to modify (and at the same time complicate) a system that is already capable of operating satisfactorily?

Furthermore, Ogita et al. teaches the use of a transformer for impedance matching—not for providing isolation between the communication antenna coil and the other circuits in the reader.

Chatelot and Ogita et al. in combination fail to teach all of the claim limitations of claim 1. Even if the references did teach all of the claim limitations of claim 1, there is no motivation for a person skilled in the art to make such a combination.

The examiner has not established the *prima facie* obviousness of claim 1.

CLAIM 2

Claim 2 reads as follows:

2. (currently amended) The reader of claim 1 wherein the transformer has a first winding and a second winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the first winding.

Neither Chatelot nor Ogita et al. disclose the configuration specified in claim 2. Nor is any motivation provided in either reference that would cause a person skilled in the art to modify Chatelot's invention in conformance with applicants' claim-2 limitations. For details, please see discussion above under the **CLAIM 1** heading.

The examiner has not established the *prima facie* obviousness of claim 2.

CLAIM 4

Claim 4 reads as follows:

4. (currently amended) The reader of claim 1 wherein the transformer has a first

winding, a second winding, and a third winding, the capacitors being connected to the first winding, the coil being connected to the second winding, and the data extractor being connected to the third winding.

Neither Chatelot nor Ogita et al. disclose the configuration specified in claim 4. Nor would a person skilled in the art be motivated to modify Chatelot's invention in conformance with applicants' claim-4 limitations. For details, please see discussion above under the **CLAIM 1** heading.

The examiner has not established the *prima facie* obviousness of claim 4.

CLAIM 41

Claim 41 reads as follows:

41. (currently amended) A tag for use with a reader, the tag comprising:

a transformer having a plurality of windings, each winding having first and second terminals;

a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

a coil driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer;

a data extractor for extracting data from the signal induced in the coil, the data extractor

having first and second terminals connected to the first and second terminals of a winding of the transformer;

a power extractor for extracting power from the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer.

The first terminals of Chatelot's capacitors 19 connect to the first and second terminals of Chatelot's transmission circuit 21 ("driver"). The second terminals of Chatelot's capacitors 19 connect to the first and second terminals of Chatelot's coil 13. Chatelot, Figs. 2 and 3.

The examiner argues that Chatelot's capacitors 19 are analogous to Ogita et al.'s capacitor 34 and Chatelot's coil 13 is analogous to Ogita et al.'s receiving antenna 11. Ogita et al., Fig. 8. The examiner then concludes that it would be obvious to one skilled in the art to combine Kurusu's transformer 17 with Chatelot's capacitors 19 and transmission coil 13 and thereby achieve applicants' claim-41 invention. Since the first terminal of Ogita et al.'s capacitor 34 is connected to the first terminal of winding 32 of transformer 31 and the second terminal of Ogita et al.'s capacitor 34 is connected to a second terminal of winding 32 of transformer 31, this arrangement with Chatelot's capacitors 19 taking the place of Ogita et al.'s capacitor results in the arrangement specified by the limitation "a capacitor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

However, the first and second terminals of Ogita et al.'s antenna 21 connect to one of the terminals of winding 32 of transformer 31 while the other connects to a tap point of winding 32. Thus, the combination of Chatelot and Ogita et al. suggested by the examiner does not disclose the

limitation "a coil having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

One terminal of Chatelot's transmission circuit 21 ("driver") connects to one terminal of Chatelot's capacitor 19 and according to the examiner's suggested combination would connect the terminal of winding 32 that the capacitor is connected to. Ogita et al. does not disclose a driver and provides no insight as to how a driver would be incorporated in his invention. The examiner has not suggested how the other terminal of Chatelot's transmission circuit 21 should be connected to a transformer winding. There is no basis for arguing that Chatelot and Ogita et al. can be combined in a way that will result in the limitation "a driver having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

One terminal of Chatelot's reception circuit 22 ("data extractor") connects to one terminal of Chatelot's capacitor 19 and according to the examiner's suggested combination would connect to the terminal of winding 32 that the capacitor is connected to. The examiner has not suggested how the other terminal of Chatelot's reception circuit 22 is to be connected. The input terminals to Ogita et al.'s amplifier 37 (corresponding to the input of a "data extractor") connect to winding 33 and have no connection to the capacitor as Chatelot requires.

The examiner has made no suggestions as to how to compatibly combine Chatelot and Ogita et al. so as to achieve an invention that includes the limitation "a data extractor for extracting data from the signal induced in the coil, the data extractor having first and second terminals connected to the first and second terminals of a winding of the transformer."

And finally, neither Chatelot nor Ogita et al. disclose circuitry, either separately or in combination, which would correspond to the limitation "a power extractor for extracting power from

the signal induced in the coil to operate the tag, the power extractor having first and second terminals connected respectively to the first and second terminals of a winding of the transformer."

Neither Chatelot nor Ogita et al. nor the references in combination disclose most of the limitations specified in claim 41. Neither Chatelot nor Ogita et al. provide motivation to a person skilled in the art to attempt a combination of Chatelot and Ogita et al. that would result in applicants' claim-41 invention.

The examiner has not established the *prima facie* obviousness of claim 41.

CLAIM 42

Claim 42 reads as follows:

42. (currently amended) The tag of claim 41 wherein the transformer has a first winding and a second winding, the capacitor, the coil driver, the data extractor, and the power extractor being connected to the first winding, the coil being connected to the second winding.

Since the references do not disclose either separately or in combination the limitations of claim 41, they obviously do not disclose the additional limitations of claim 42 which depends from claim 41. The references also do not provide any motivation to a person skilled in the art to combine the references for the purpose of achieving an invention with the limitations of claim 42.

The examiner did not address the specific limitations of claim 42 in either of his office actions and has not established the *prima facie* obviousness of claim 42.

CLAIM 44

Claim 44 reads as follows:

44. (currently amended) The tag of claim 41 wherein the transformer has a first winding, a second winding, and a third winding, the capacitor and the coil driver being connected to the first winding, the data extractor and the power extractor being connected to the second winding, and the coil being connected to the third winding.

Since the references do not disclose either separately or in combination the limitations of claim 41, they obviously do not disclose the additional limitations of claim 44 which depends from claim 41. The references also do not provide any motivation to a person skilled in the art to combine the references for the purpose of achieving an invention with the limitations of claim 44.

The examiner did not address the specific limitations of claim 44 in either of his office actions and has not established the *prima facie* obviousness of claim 44.

CLAIM 45

Claim 45 reads as follows:

45. (currently amended) The tag of claim 41 wherein the transformer has a first winding, a second winding, a third winding, and a fourth winding, the capacitor and the coil driver being connected to the first winding, the data extractor being connected to the second winding, the power extractor being connected to the third winding, and the coil being connected to the fourth winding.

Since the references do not disclose either separately or in combination the limitations of claim 41, they obviously do not disclose the additional limitations of claim 45 which depends from claim 41. The references also do not provide any motivation to a person skilled in the art to combine the references for the purpose of achieving an invention with the limitations of claim 45.

The examiner did not address the specific limitations of claim 45 in either of his office actions and has not established the *prima facie* obviousness of claim 45.

VIII. WHETHER CLAIMS 5-13, 25-31, 47-60, 62-64 AND 69 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194).

CLAIM 5

Claim 5 reads as follows:

5. A reader for use with a tag, the reader comprising:

a coil;

[1] at least one capacitor;

[2] a means for coupling the capacitor(s) to the coil;

[3] a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

[4] a means for embedding a bit-timing clock signal in the driving signal;

a means for embedding a sequence of bits to be communicated to a tag in the driving signal.

Carroll et al. does not disclose any of the limitations shown in boldface above.

Limitations [1], [2], and [3]

Carroll et al. utilizes microprocessor 12 to directly drive coil 18 by means of coil drive circuit 16. No capacitor is involved in the process. Carroll et al., col. 6, lines 7-9. Thus, Carroll et al. does not disclose limitations [1], [2], and [3].

The examiner argues that it would be obvious to a person skilled in the art to incorporate Carroll et al.'s tuning capacitor 44 in transponder 40 (Carroll et al., Fig. 3) as a feed-through capacitor from coil drive 16 to coil 18 in controller 10 (Carroll et al., Fig. 1) in order to provide tuning.

Carroll et al. were obviously aware of the use of a tuning capacitor as they demonstrated by incorporating a tuning capacitor at the front end of their transponder. And yet Carroll et al. did not see the need or the desirability of incorporating such a capacitor in their controller 10. In fact, the design of controller 10 seems to have been more than adequate for their purposes: "Utilizing the combination of FSK and PSK modulation techniques, in conjunction with a ferroelectric memory array, allows the transponder "write" range to be the same as the "read" range and precludes interference between read and write commands or other transponders which may be within the RF signal range of the controller." Carroll et al., col. 2, lines 45-51. If the inventors did not recognize a need or the desirability of incorporating a tuning capacitor in controller 10, is it likely that a person skilled in the art would come to the opposite conclusion?

Limitation [4]

Please see the discussion under the **ISSUE V, CLAIM 70** heading for an argument in support of the assertion that Carroll et al. does not disclose Limitation [4], "a means for embedding a bit-timing clock signal in the driving signal."

Carroll et al. does provide a means for embedding a bit-timing clock signal in the signal returned by transponder 40 to controller 10. However, there is no basis for arguing that a person skilled in the art would find it obvious to also embed a bit-timing clock signal in the driving signal transmitted by controller 10 to transponder 40. Again, Carroll et al. were undoubtedly aware of this option and chose not to do it. It is unlikely that a person skilled in the art would come to an opposite conclusion.

Carroll et al. does not "teach or suggest all the claim limitations" of claim 5 and prima facie obviousness of claim 5 has not been established.

CLAIM 6

Claim 6 reads as follows:

6. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal. Controller 10 embeds a sequence of bits in the driving signal by changing the frequency of the

driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not a teaching of the claim-6 limitation.

The examiner seems to argue that because Carroll et al.'s transponder 40 responds to controller 10's interrogation with a PSK signal, a person skilled in the art would be motivated to change controller 10's means for communicating data to transponder 40 to PSK. However, there is no suggestion in Carroll et al. or in the knowledge generally available to one of ordinary skill in the art to make such a change. Carroll et al. chose the simple means of varying the frequency of the driving signal for communicating data from controller 10 to transponder 40 because the detection of frequency changes is particularly simple and does not require a bit-timing clock signal to be available in transponder 40 thereby resulting in a less-complicated and less-costly transponder.

There is no motivation for changing controller 10's method of transmitting data to transponder 40, and consequently, prima facie obviousness of applicants' claim-6 invention has not been established.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s preferred FSK mode of communication from controller 10 to transponder 40 to PSK, the examiner made the following statement:

> "While Carroll does in fact teach using FSK to communicate data to the tag, Carroll also teaches the use of PSK to transmit data. It is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods. Does the applicant actually believe that they invented the use of PSK in a communication?" 08/12/03 Office Action, p. 22.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation:

> **"At best, the examiner's comments regarding obviousness amount to an assertion that one of ordinary skill in the relevant art would have been able to arrive at appellant's invention because he had the necessary skills to carry out the requisite process steps. This is an inappropriate standard for obviousness. See *Orthokinetics Inc. v. Safety Travel Chairs Inc.*, 806 F.2d 1565, 1 USPQ2d 1081 (Fed. Cir. 1986). That which is within the capabilities of one skilled in the art is not synonymous with obviousness. *Ex parte Gerlach*, 212 USPQ 471 (Bd.App. 1980). See also footnote 16 of *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 1092, 227 USPQ 337, 343 (Fed. Cir. 1985)."** *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

CLAIM 7

Claim 7 reads as follows:

7. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 7.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal.

Carroll et al. does not teach the limitation of claim 7, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 7 has not been established.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 08/12/03 Office Action, p. 22.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

CLAIM 8

Claim 8 reads as follows:

8. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 8.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to amplitude modulate the driving signal.

Carroll et al. does not teach the limitation of claim 8, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 8 has not been established.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 08/12/03 Office Action, p. 22.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

CLAIM 9

Claim 9 reads as follows:

9. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 9.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to phase modulate the driving signal.

Carroll et al. does not teach the limitation of claim 9, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 9 has not been established.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 08/12/03 Office Action, p. 22.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

CLAIM 10

Claim 10 reads as follows:

10. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 10.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as "causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted" .

Carroll et al. does not teach the limitation of claim 10, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 10 has not been established.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 08/12/03 Office Action, p. 22.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

CLAIM 11

Claim 11 reads as follows:

11. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 11.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 11, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 11 has not been established.

In response to applicants' arguments that motivation is lacking for changing Carroll et al.'s mode of communication from controller 10 to transponder 40, the examiner argues that "[i]t is well within the skill in the art to choose between transmission encoding schemes to provide optimal transmission methods." 08/12/03 Office Action, p. 22.

The fact that "it is well within the skill in the art to choose transmission encoding schemes" does not qualify as motivation. *Ex parte Levengood*, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Inter. 1993.

CLAIM 12

Claim 12 reads as follows:

12. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 12.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic

signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude-modulating the driving signal with this periodic signal.

The examiner ignores the differences in the frequency modulation claimed by applicants and the frequency modulation disclosed by Carroll et al. and concludes:

"What the applicant claims is FSK. Carroll discloses FSK for the claimed link between the reader and the tag." 08/12/03 Office Action, pp. 22-23.

The examiner is incorrect in substituting his interpretation of the claim language for the actual claim language. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

Carroll et al. does not teach the limitation of claim 12, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 12 has not been established.

CLAIM 13

Claim 13 reads as follows:

13. The reader of claim 5 wherein the means for embedding a sequence of bits comprises: a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 13.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

The examiner ignores the differences in the frequency modulation claimed by applicants and the frequency modulation disclosed by Carroll et al. and concludes:

> "What the applicant claims is FSK. Carroll discloses FSK for the claimed link between the reader and the tag." 08/12/03 Office Action, pp. 22-23.

The examiner is incorrect in substituting his interpretation of the claim language for the actual claim language. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

Carroll et al. does not teach the limitation of claim 13, and there is no motivation for changing controller 10's method of transmitting data to transponder 40.

Prima facie obviousness of claim 13 has not been established.

CLAIM 25

Claim 25 reads as follows:

*25. A reader for use with **[1] a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated**, the reader comprising:*

a means for receiving the tag signal;

[2] a means for measuring the period of each cycle of the signal received from the tag during a bit period.

Carroll et al. does not teach either of the limitations shown in boldface.

Limitation [1]

Carroll et al. discloses controller 10 which can be used with transponder 40 which utilizes a phase-coherent Manchester encoded PSK RF signal to send data. Carroll et al., col. 15, lines 54-56. Carroll et al. does not teach a reader that can be used with "a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated."

The examiner ignores the differences in the frequency modulation claimed by applicants and the frequency modulation disclosed by Carroll et al. and concludes:

"What the applicant claims is FSK. Carroll discloses FSK for the claimed link between the reader and the tag." 08/12/03 Office Action, pp. 22-23.

The examiner is incorrect in substituting his interpretation of the claim language for the actual claim language. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

The examiner argues that a preamble limitation is "generally not accorded any patentable weight where it merely recites the purpose of a process or the intended used of a structure and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 08/12/03 Office Action, p. 13.

Limitation [1] does not merely recite an intended use of the reader. The primary function of a reader is to "read" the data transmitted by a tag. To do this, the structure of the reader must be tailored to the method used by the tag to transmit data. Thus, limitation [1] is clearly a limitation on the structure of the reader that cannot be ignored.

Limitation [2]

Carroll et al.'s controller 10 anticipates receiving a phase-modulated 62.5-kHz signal from transponder 40 (Carroll et al., Fig. 3). Carroll et al. does not need to measure the period of the received signal nor does it disclose performing such an operation

Carroll et al. does not teach the limitations of claim 25, and there is no motivation for changing controller 10's method of receiving data from transponder 40.

Prima facie obviousness of claim 25 has not been established.

CLAIM 26

Claim 26 reads as follows:

26. The reader of claim 25 further comprising:

a means for identifying the bit transmitted by the tag from the measurements of the period of each cycle of the signal received from the tag during a bit period.

Carroll et al. does not teach the limitation of claim 26, and there is no motivation for incorporating the limitation in Carroll et al.'s controller 10.

Prima facie obviousness of claim 26 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."

08/12/03 Office Action, p. 23.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has

failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action:

"(A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate,

"(B) The difference or differences in the claim over the applied references(s),

"(C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and

"(D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 27

Claim 27 reads as follows:

27. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

Carroll et al. does not teach the limitation of claim 27, and there is no motivation for incorporating the limitation in Carroll et al.'s controller 10.

Prima facie obviousness of claim 27 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."
>
> 08/12/03 Office Action, p. 23.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the

applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 28

Claim 28 reads as follows:

28. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

Carroll et al. does not teach the limitation of claim 28, and there is no motivation for incorporating the limitation in Carroll et al.'s controller 10.

Prima facie obviousness of claim 28 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 08/12/03 Office Action, p. 23.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 29

Claim 29 reads as follows:

29. The reader of claim 25 further comprising:

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change greater than a predetermined value in the period of a cycle from one cycle to the next cycle.

Carroll et al. does not teach the limitation of claim 29, and there is no motivation for incorporating the limitation in Carroll et al.'s controller 10.

Prima facie obviousness of claim 29 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."
>
> 08/12/03 Office Action, p. 23.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the

applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 30

Claim 30 reads as follows:

30. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

Carroll et al. does not teach the limitation of claim 30, and there is no motivation for incorporating the limitation in Carroll et al.'s controller 10.

Prima facie obviousness of claim 30 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 08/12/03 Office Action, p. 23.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 31

Claim 31 reads as follows:

31. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if

the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

Carroll et al. does not teach the limitation of claim 31, and there is no motivation for incorporating the limitation in Carroll et al.'s controller 10.

Prima facie obviousness of claim 31 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."
>
> 08/12/03 Office Action, p. 23.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference

or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 47

Claim 47 reads as follows:

47. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, ***[1] the reader embedding a bit-timing clock signal in the transmitted signals****, the tag comprising:*

a coil;

a capacitor;

a means for coupling the capacitor to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the combination of the coil, the capacitor, and the coupling means being called the resonating circuit;

[2] a means for generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the transmitted signals;

[3] a means for identifying the bit being transmitted during each bit period, the beginning and ending of each bit period being indicated by the bit-timing clock signal.

Carroll et al. does not disclose any of the limitations in boldface.

Limitation [1]

Limitation [1] is not disclosed by Carroll et al. For details, please see discussion under the **ISSUE V, CLAIM 70** heading.

The examiner argues that a preamble limitation is "generally not accorded any patentable weight where it merely recites the purpose of a process or the intended used of a structure and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 08/12/03 Office Action, p. 13.

Limitation [1] does not merely recite an intended use of the tag. One of the primary functions of a tag is to "read" the data transmitted by a reader. To do this, the structure of the tag must be tailored to the method used by the reader to transmit data. Thus, limitation [1] is clearly a limitation on the structure of the tag that cannot be ignored.

Limitation [2]

Carroll et al.'s controller 10 does not transmit a bit-timing clock signal to transponder 40 (see discussion under **ISSUE V, CLAIM 70** heading). Consequently, there is no bit-timing clock signal originating in controller 10 that could be used by transponder 40 to synchronize its own bit-timing clock. For additional discussion of this limitation, see **ISSUE V, CLAIM 74, *Limitation [2].***

Carroll et al. does not teach Limitation [2].

Limitation [3]

Carroll et al.'s transponder 40 has no information available from controller 10 as to the beginning and ending of a bit period and therefore does not teach the use of this information in identifying the bit being transmitted during the bit period.

The examiner argues that "[t]he sync generator 70 is synchronized to the received clock signal since the timing control element 60 drives all the elements that follow, etc 64,48,68 and 70." 08/12/03 Office Action, p. 18. The "received clock signal" that the examiner refers to is presumably the FSK modulated signal of frequency 125 kHz from controller 10. col. 7, lines 22-25; col. 17, lines 39-52. This is the carrier of the data that controller 10 transmits to transponder 40. It is not a bit-timing clock signal to which the bit-timing clock signal generated by transponder 40 is synchronized.

Carroll et al. does not teach Limitation [3].

Carroll et al. does not teach the boldface limitations of claim 47, and there is no motivation for incorporating the limitations in Carroll et al.'s controller 10 and transponder 40.

Prima facie obviousness of claim 47 has not been established.

CLAIM 48

Claim 48 reads as follows:

48. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-48 limitation.

Carroll et al. does not teach the limitation of claim 48, and there is no motivation for incorporating the limitation in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 48 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."
>
> 08/12/03 Office Action, p. 23-24.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitation is not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why

one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 49

Claim 49 reads as follows:

49. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

The examiner argues that "amplitude shift keying is a common alternative to phase shift keying or frequency shift keying, and to have substituted this type of modulation scheme for that used in Carroll would not have involved an unobvious step." 08/12/03 Office Action, p. 9. There is no mention of amplitude shift keying in claim 49 or in claim 47 from which claim 49 depends. It would appear that the examiner's comment is irrelevant insofar as the patentability of applicants' claim-49 invention is concerned.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-49 limitations. The examiner argues that [d]ividing by 64 is weighted integration for providing the claimed feature. 08/12/03 Office Action, p. 24. The divide-by-64 timing control 60 is simply a synchronous counter (col. 18, lines 58-60). It has nothing to do with performing a weighted integration of a received signal. A weighted

integration results from the multiplication of the signal received during a bit period by a weighting function and integrating the result.

Carroll et al. does not teach the limitations of claim 49, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 49 has not been established.

CLAIM 50

Claim 50 reads as follows:

50. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

Carroll et al. does not even mention the term "weighted integration" let alone teaching its use in determining bit values in accordance with the claim-50 limitations. The examiner argues that [d]ividing by 64 is weighted integration for providing the claimed feature. 08/12/03 Office Action, p. 24. The divide-by-64 timing control 60 is simply a synchronous counter (col. 18, lines 58-60). It has nothing to do with performing a weighted integration of a received signal. A weighted integration results from the multiplication of the signal received during a bit period by a weighting function and integrating the result.

Carroll et al. does not teach the limitations of claim 50, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 50 has not been established.

CLAIM 51

Claim 51 reads as follows:

51. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter;

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

Carroll et al. does not teach either of the limitations in boldface, and there is no motivation for incorporating the limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 51 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitation in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate such a limitation in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 08/12/03 Office Action, p. 24.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations in boldface are not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitations.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 52

Claim 52 reads as follows:

52. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal;

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

Carroll et al. does not teach any of the limitations of claim 52 (i.e. all limitations shown in boldface), and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 48 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of the limitations in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate these limitations in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 08/12/03 Office Action, p. 23-24.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations are not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include these limitations.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 53

Claim 53 reads as follows:

53. The tag of claim 47 wherein the bit-identifying means comprises:

a means for generating replicas of the first and second signals transmitted by the reader;

a means for obtaining the amplitude of a coupling-means signal as a function of time;

a means for multiplying the coupling-means signal amplitude by the replica of the first signal to obtain a first product signal and by the replica of the second signal to obtain a second product signal;

a means for integrating the first product signal over a bit period to obtain a first integration and integrating the second product signal over a bit period to obtain a second integration;

a means for translating the first and second integrations into a bit value.

Carroll et al. does not teach the limitations of claim 53 shown in boldface, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 53 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of these limitations in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate these limitations in Carroll et al.'s invention by stating:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."

08/12/03 Office Action, p. 23-24.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations in boldface are not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitations.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 54

Claim 54 reads as follows:

54. The tag of claim 47 wherein the means for generating a bit-timing clock signal that indicates the start of each bit period comprises:

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transition in the coupling-means signal from one bit to the next;

a means for adjusting the bit-start indicators until the bit-start indicators and the bit transitions in the coupling-means signal occur simultaneously.

Carroll et al. does not teach the limitations of claim 54 shown in boldface, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 54 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of these limitations in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate these limitations in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references."
>
> 08/12/03 Office Action, p. 23-24.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations in boldface are not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include these limitations.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the

applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 55

Claim 55 reads as follows:

55. The tag of claim 47 wherein ***the reader embeds a bit-timing clock signal in the transmitted signals by initially alternating the transmission of the first signal and the second signal,*** *the means for generating a bit-timing clock signal that indicates the start of each bit period comprising:*

a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

a means for recognizing the bit transitions in the coupling-means signal resulting from the transitions from the first signal to the second signal and from the second signal to the first signal;

a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal occur simultaneously.

Carroll et al. does not teach the limitations of claim 55 shown in boldface, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 55 has not been established.

The examiner responded to applicants' assertion that there is no disclosure of these limitations in Carroll et al. and that there is no motivation for a person skilled in the art to incorporate these limitations in Carroll et al.'s invention by stating:

> "Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." 08/12/03 Office Action, p. 23-24.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations shown in boldface are not disclosed in the reference. And in two office actions, the examiner has failed to rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include these limitations.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

CLAIM 56

Claim 56 reads as follows:

56. A tag for use with a reader, ***[1] the reader transmitting a bit-timing clock signal to the tag,*** *the tag comprising:*

a coil;

a capacitor;

a means for coupling the capacitor to the coil;

a means for driving the coil with a driving signal;

a means for generating the driving signal;

[2] a means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal;

[3] a means for embedding a sequence of bits to be communicated to a reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal.

Carroll et al. does not teach the limitations of claim 56 shown in boldface, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Limitation [1]

Limitation [1] is not disclosed by Carroll et al. For details, please see discussion under the **ISSUE V, CLAIM 70** heading.

The examiner argues that a preamble limitation is "generally not accorded any patentable weight where it merely recites the purpose of a process or the intended used of a structure and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone." 08/12/03 Office Action, p. 13.

Limitation [1] does not merely recite an intended use of the tag. One of the primary functions of a tag is to "read" the data transmitted by a reader. To do this, the structure of the tag must be tailored to the method used by the reader to transmit data. Thus, limitation [1] is clearly a limitation on the structure of the tag that cannot be ignored.

Limitation [2]

Carroll et al.'s controller 10 does not transmit a bit-timing clock signal to transponder 40 (see discussion under **ISSUE V, CLAIM 70** heading). Consequently, there is no bit-timing clock signal originating in controller 10 that could be used by transponder 40 to synchronize its own bit-timing clock. For additional discussion of this limitation, see **ISSUE V, CLAIM 74, *Limitation [2].***

Carroll et al. does not teach Limitation [2].

Limitation [3]

Since the bit-timing clock signal specified by limitation [2] does not exist in Carroll et al.'s transponder 40, Carroll et al. obviously cannot disclose limitation [3] which requires this non-existent bit-timing clock signal.

Carroll et al. does not teach the boldface limitations of claim 56, and there is no motivation for incorporating these limitations in Carroll et al.'s transponder 40.

Prima facie obviousness of claim 56 has not been established.

The examiner argues that "Carroll is not cited for teaching each and every element as claimed" (08/12/03 Office Action, p. 24) and yet he cites no other references. The examiner argues

that "applicant failed to appreciate the teachings of Carroll" (08/12/03 Office Action, p. 24). But pointing out that Carroll et al. does not disclose specified limitations in claims does not mean that applicants "failed to appreciate the teachings of Carroll." Finally, the examiner argues that "applicant ignored the application of Carroll as discussed in the OBVIOUSNESS rejection set forth in the Office Action" (08/12/03 Office Action, p. 24) but applicants are unable to find any discussion whatsoever of claim 56 and its limitations in the "obviousness" portion of the office action relating to Carroll et al. See 08/12/03 Office Action, pp. 7-8.

CLAIM 57

Claim 57 reads as follows:

57. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

Carroll et al. teach the use of Manchester coded PSK in transmitting data from transponder 40 (analogous to applicants' tag) to controller 10. Carroll et al., col. 20, lines 33-35. Manchester-coded PSK results in the driving signal having (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) a second phase during the first half of a bit period and a first phase during the second half of a bit period when a "1" is transmitted. Manchester-coded PSK is not a teaching of applicants' claim-57 limitation.

Manchester-coded PSK has some very desirable properties, and a person skilled in the art would not be motivated by knowledge generally available to one of ordinary skill in the art to change Carroll et al.'s modulation technique to the one specified in applicants' claim 57.

Carroll et al. does not teach the claim-57 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 57. *Prima facie* obviousness of claim 57 has not been established.

The examiner argues that the claim language does not require "the phase be constant for the entire bit period." 08/12/03 Office Action, p. 25.

The examiner wants to interpret "a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted" as meaning "a means for causing the phase of the driving signal to have a first phase FOR AT LEAST A PORTION OF THE TIME when a "0" bit is being transmitted." But the words "FOR AT LEAST A PORTION OF THE TIME" do not appear in the claim.

Would the examiner also argue that the statement "the horn sounds when the horn button is being pushed" actually means "the horn sounds FOR AT LEAST A PORTION OF THE TIME when the horn button is being pushed"? More likely, the latter would be attributed to a malfunctioning horn circuit.

The language does require the phase of the driving signal to be a constant during the entire bit period and to be equal to a "first phase" when a "0" bit is being transmitted and to be equal to a "second phase" when a "1" bit is being transmitted. This interpretation of "phase" is consistent with the definition "an additive constant in the argument of a trigonometric function." McGraw-Hill

Dictionary of Scientific and Technical Terms, Fourth Edition, McGraw-Hill, Inc., New York, N.Y. (1989).

CLAIM 58

Claim 58 reads as follows:

58. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 58.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to modulate the driving signal.

Carroll et al. does not teach the claim-58 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 58. *Prima facie* obviousness of claim 58 has not been established.

The examiner argues that the claim language does not require the phase to be constant for the entire bit period. 08/12/03 Office Action, pp. 24-25. Please see discussion under the **CLAIM 57** heading above.

CLAIM 59

Claim 59 reads as follows:

59. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 59.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to amplitude modulate the driving signal.

Carroll et al. does not teach the claim-59 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 59. *Prima facie* obviousness of claim 59 has not been established.

The examiner argues that the claim language does not require the phase to be constant for the entire bit period. 08/12/03 Office Action, pp. 24-25. Please see discussion under the **CLAIM 57** heading above.

CLAIM 60

Claim 60 reads as follows:

60. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 60.

Carroll et al.'s controller 10 transmits data by changing the frequency of the driving signal. Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al., col. 3, lines 45-62. This is not the same as generating "a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted" and then using this "periodic signal" to phase modulate the driving signal.

Carroll et al. does not teach the claim-60 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 60. *Prima facie* obviousness of claim 60 has not been established.

The examiner argues that the claim language does not require the phase to be constant for the entire bit period. 08/12/03 Office Action, pp. 24-25. Please see discussion under the **CLAIM 57** heading above.

CLAIM 62

Claim 62 reads as follows:

62. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 62.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then modulating the driving signal with this periodic signal.

Carroll et al. does not teach the limitation of claim 62, and consequently, prima facie obviousness of claim 62 has not been established.

Carroll et al. does not teach the claim-62 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 62. *Prima facie* obviousness of claim 62 has not been established.

The examiner argues that "[c]laim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1", this is the definition of FSK which is shown by Carroll." 08/12/03 Office Action, p. 25. What the examiner seems to be saying is that the claim-62 and Carroll et al.'s modulation techniques are simply different types of FSK and the differences can be ignored. The differences are substantial and cannot be ignored. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

CLAIM 63

Claim 63 reads as follows:

63. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 63.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then amplitude modulating the driving signal with this periodic signal.

Carroll et al. does not teach the claim-63 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 63. *Prima facie* obviousness of claim 63 has not been established.

The examiner argues that "[c]laim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1", this is the definition of FSK which is shown by Carroll." 08/12/03 Office Action, p. 25. This argument would also seem to apply to claim 63. What the examiner seems to be saying is that the claim-62 (or claim 63) and Carroll et al.'s modulation techniques are simply different types of FSK and the differences can be ignored. The differences are substantial and cannot be ignored. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

CLAIM 64

Claim 64 reads as follows:

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 64.

Carroll et al.'s transponder 40 transmits data by reversing the phase of the driving signal in accordance with the bits to be transmitted. Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29. This is not the same as generating "a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted" and then phase modulating the driving signal with this periodic signal.

Carroll et al. does not teach the claim-64 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 64. *Prima facie* obviousness of claim 64 has not been established.

The examiner argues that "[c]laim 62 for example modulates the driving signal with a first frequency to represent a "0" and modulates with a second frequency to represent a "1", this

is the definition of FSK which is shown by Carroll." 08/12/03 Office Action, p. 25. This argument would also seem to apply to claim 64. What the examiner seems to be saying is that the claim-62 (or claim-64) and Carroll et al.'s modulation techniques are simply different types of FSK and the differences can be ignored. The differences are substantial and cannot be ignored. All of the words in the claim must be considered:

> **"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970)." MPEP § 2143.03.**

CLAIM 69

Claim 69 reads as follows:

69. The tag of claim 56 wherein the reader transmits the bit-timing clock signal to the tag by communicating a sequence of alternating "0" and "1" bits, a "0" bit being communicated by modulating the amplitude of the driving signal with a first periodic signal, a "1" bit being communicated by modulating the amplitude of the alternating field with a second periodic signal, ***[claim-56 limitation] the means for generating the clock signal that is synchronized to the bit-timing signal transmitted by the reader to the tag*** *comprising:*

[1] a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;

[2] a means for obtaining the amplitude of a coupling-means signal as a function of time;

[3] a means for recognizing the transitions in the coupling-means signal amplitude at the time interfaces of the first and second periodic signals;

[4] a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal amplitude occur simultaneously.

As the claim states, the means shown in boldface in the preamble, a claim-56 limitation, is comprised of limitations [1], [2], [3], and [4]. None of these limitations are taught by Carroll et al.

Carroll et al. does not teach the claim-64 limitations, and there is no motivation for incorporating these limitations in claim 69. *Prima facie* obviousness of claim 69 has not been established.

The examiner argues that "Carroll is not cited for teaching each and every element as claimed" (08/12/03 Office Action, p. 25) and yet he cites no other references. The examiner argues that "applicant failed to appreciate the teachings of Carroll" (08/12/03 Office Action, p. 25). But pointing out that Carroll et al. does not disclose specified limitations in claims does not mean that applicants "failed to appreciate the teachings of Carroll." Finally, the examiner argues that "applicant ignored the application of Carroll as discussed in the OBVIOUSNESS rejection set forth in the Office Action" (08/12/03 Office Action, p. 25) but applicants are unable to find any discussion whatsoever of claim 69 and its limitations in the "obviousness" portion of the office action relating to Carroll et al. See 08/12/03 Office Action, pp. 7-8.

The examiner also states:

"Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Repeating the claim and arguing, ' the references do not show the claimed subject matter' amounts to a general allegation." 08/12/03 Office Action, p. 225.

Applicants' argument is not a general allegation. The argument is very specific in stating that the claim limitations are not disclosed in the reference. And in two office actions, the examiner has failed to cite disclosures and/or rebut applicants' argument. Moreover, the examiner has not established motivation on the part of a person skilled in the art to modify the referenced invention to include the limitation.

The examiner is reminded that in rejecting a claim for obviousness, he "should set forth in the Office action (A) The relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate, (B) The difference or differences in the claim over the applied references(s), (C) The proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification." MPEP § 706.02(j).

IX. WHETHER CLAIMS 34 AND 35 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF WARAKSA (U.S. 4,942,393) AND BATZ ET AL. (U.S. 4,839,642).

CLAIM 34

Claim 34 reads as follows:

34. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits;

a means for determining whether the oldest S bits in memory is a sync sequence;

[1] a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

[2] a control means for causing the determining means and the replacing means to operate alternately after the memory is filled with received bits.

Neither Waraksa et al. nor Batz et al. teach the limitations shown in boldface.

The tag of applicants' invention, after it is interrogated by a reader, continually transmits a repeated message consisting of S sync bits, T tag data bits, and T error-detecting bits. The reader, by the time it is ready to extract data from the tag's transmission, may begin obtaining data in the middle of a message. In order to detect errors and extract the tag data from the message, it must first identify the sync bits. It does this by storing the bits as they arrive and continually examining the oldest S bits to determine whether they correspond to the sync sequence. If they do not, the oldest bit is discarded and the "new" oldest S bits is examined. This process is repeated until the sync bits are discovered.

Neither of the references cited by the examiner teach this process. The examiner argues that Batz et al. discloses the claim-34 limitations and cites col. 14, lines 42+. But the first line of the cited passage reveals that there is no uncertainty in the Batz et al. interrogation as to the identity of the sync bits: "The sync word shift register 225 receives and decodes the first eight bits which correspond to the sync word portion of the incoming interrogate signal." Batz et al., col. 14, lines 43-45. There is no uncertainty in the Batz et al. system as to which bits in the received interrogation

correspond to the sync word. The sync word consists of the first eight bits received. The primary concern in the Batz et al. system is that a responder only responds to an interrogation having a valid sync word.

Limitation [1]

Batz et al. does not disclose "replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits". Batz et al. simply wait until the first eight bits of an interrogation message has been received and then determines whether this eight-bit "received" sync word corresponds to a stored sync word. If it is not, the interrogation cycle ends. Batz et al., col. 4, lines 35-38.

The examiner had no response to this argument in his 08/12/03 Office Action.

Limitation [2]

Batz et al. does not disclose "causing the determining means and the replacing means to operate alternately after the memory is filled with received bits". Batz et al.'s "determining means" which determines whether the oldest S bits in memory is a sync sequence operates only once immediately after the first 8 bits of the interrogation message is received. Batz et al., col.4, lines 6-53.

The examiner had no response to this argument in his 08/12/03 Office Action.

Neither Waraksa et al. nor Batz et al. teaches the claim-34 limitations, and there is no motivation for modifying Waraksa et al.'s invention to include these limitations.

Prima facie obviousness of claim 34 has not been established.

CLAIM 35

Claim 35 reads as follows:

35. The reader of claim 33 wherein the sync sequence detecting means comprises: a memory for storing (S+T+E) received data bits;

[1] a first means for determining whether the newest S bits in memory is a sync sequence;

[2] a second means for determining whether the oldest S bits in memory is a sync sequence;

[3] a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

[4] a control means for causing the first determining means and the replacing means to operate alternately until a sync sequence is detected, the control means causing the second determining means and the replacing means to operate alternately if a detected sync sequence is determined to be a false-sync sequence.

Neither Waraksa et al. nor Batz et al. teach the limitations shown in boldface.

The tag of applicants' invention, after it is interrogated by a reader, continually transmits a repeated message consisting of S sync bits, T tag data bits, and T error-detecting bits. The reader, by the time it is ready to extract data from the tag's transmission, may begin obtaining data in the middle of a message. In order to detect errors and extract the tag data from the message, it must first identify the sync bits. It does this by storing the bits as they arrive and continually examining the

oldest S bits to determine whether they correspond to the sync sequence. If they do not, the oldest bit is discarded and the "new" oldest S bits is examined. This process is repeated until the sync bits are discovered.

Neither of the references cited by the examiner teach this process. The examiner argues that Batz et al. discloses the claim-35 limitations and cites col. 14, lines 42+. But the first line of the cited passage reveals that there is no uncertainty in the Batz et al. interrogation as to the identity of the sync bits: "The sync word shift register 225 receives and decodes the first eight bits which correspond to the sync word portion of the incoming interrogate signal." Batz et al., col. 14, lines 43-45. There is no uncertainty in the Batz et al. system as to which bits in the received interrogation correspond to the sync word. The sync word consists of the first eight bits received. The primary concern in the Batz et al. system is that a responder only responds to an interrogation having a valid sync word.

Limitations [1] and [2]

Batz et al. does not envision a situation where the identification of a sync sequence involves both a determination as to whether the newest S bits is a sync sequence and a determination as to whether the oldest S bits in memory is a sync sequence. Batz et al. is only concerned with the first-arriving eight bits. Batz et al., col. 4, lines 35-37.

The examiner had no response to this argument in his 08/12/03 Office Action.

Limitation [3]

Batz et al. does not disclose "replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits". Batz et al. simply wait until the first eight bits of an interrogation message has been received and then determines whether this eight-bit "received" sync word corresponds to a stored sync word. If it is not, the interrogation cycle ends. Batz et al., col. 4, lines 35-38.

The examiner had no response to this argument in his 08/12/03 Office Action.

Limitation [4]

There is nothing in Batz et al. that teaches this limitation.

The examiner had no response to this argument in his 08/12/03 Office Action.

Neither Waraksa et al. nor Batz et al. teaches the claim-35 limitations, and there is no motivation for modifying Waraksa et al.'s invention to include these limitations.

Prima facie obviousness of claim 35 has not been established.

X. WHETHER CLAIMS 14-17, 61, AND 64-68 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(A) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194) AND MCFARLANE (U.S. 3,223,779).

CLAIM 14

Claim 14 reads as follows:

14. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to the PHASE of a driving signal. Thus, McFarlane does not teach the limitation of claim 15.

Carroll et al. utilize a simple FSK technique for communicating commands from controller 10 to transponder 40 where the controller 10 is constructed around a commercially-available microcomputer chip. Carroll et al., col. 5, line 64 - col. 6, line 16. The extraction of data from the received signal by transponder 40 is accomplished by a simple circuit consisting of an oscillator, an up/down counter, and logic circuits. Carroll et al., col. 18, lines 44-57. McFarlane discloses a combined FSK/PSK communication technique which involves at the transmit end two frequency multipliers, two phase shifters, logic circuitry, and an analog signal combiner. McFarlane discloses data extraction circuitry at the receive end consisting of two filters, four frequency multipliers, four frequency dividers, two phase detectors, and associated logic circuitry. McFarlane, Fig. 1.

Even if the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s FSK circuitry would result in a reader with the limitations of claim 14 (which it would NOT), there is no motivation for such a modification.

The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-14 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique.

The examiner has not established *prima facie* obviousness of applicants' claim-14 invention.

CLAIM 15

Claim 15 reads as follows:

15. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-15 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 15.

The references do not disclose the claim-15 limitation nor do the references provide motivation for making a change in Carroll et al.'s controller 10 modulation technique. Please see discussion under the **CLAIM 14** heading for additional details.

The examiner has not established *prima facie* obviousness of applicants' claim-15 invention.

CLAIM 16

Claim 16 reads as follows:

16. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-16 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this

modulated periodic signal to amplitude modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 16.

The references do not disclose the claim-16 limitation nor do the references provide motivation for making a change in Carroll et al.'s controller 10 modulation technique. Please see discussion under the **CLAIM 14** heading for additional details.

The examiner has not established *prima facie* obviousness of applicants' claim-16 invention.

CLAIM 17

Claim 17 reads as follows:

17. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-17 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 17.

The references do not disclose the claim-17 limitation nor do the references provide motivation for making a change in Carroll et al.'s controller 10 modulation technique. Please see discussion under the **CLAIM 14** heading for additional details.

The examiner has not established *prima facie* obviousness of applicants' claim-17 invention.

CLAIM 61

Claim 61 reads as follows:

61. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

Neither Carroll et al. nor McFarlane disclose a modulation technique wherein the PHASE of the driving signal has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. This is NOT the same as a modulation technique wherein the DRIVING SIGNAL has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted.

Carroll et al. teach the use of Manchester coded PSK in transmitting data from transponder 40 (analogous to applicants' tag) to controller 10. Carroll et al., col. 20, lines 33-35. Manchester-coded PSK results in the driving signal having (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) the second phase during the first half of a bit period and the first phase during the second half of a bit period when a "1" is transmitted.

Manchester-coded PSK has some very desirable properties, and a person skilled in the art would not be motivated by knowledge generally available to one of ordinary skill in the art to change Carroll et al.'s modulation technique to the one specified in applicants' claim 61.

Neither of the references teaches the claim-61 limitation, and there is no motivation for changing Carroll et al.'s preferred modulation technique to the one specified in claim 61. The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-61 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique.

The examiner has not established *prima facie* obviousness of applicants' claim-61 invention.

CLAIM 64

Claim 64 reads as follows:

64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

Neither Carroll et al. nor McFarlane disclose a modulation technique wherein the PHASE of the driving signal is modulated by a PERIODIC signal having a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted. This is NOT the same as a modulation technique wherein the DRIVING SIGNAL has a first frequency when a "0" bit is being transmitted and a second frequency when a "1" bit is being transmitted.

Neither Carroll et al.'s controller 10 nor transponder 40 utilizes the communication technique specified in claim 64.

Carroll et al.'s controller 10 interrogates transponder 40 by transmitting a driving signal wherein a sequence of bits is embedded in the driving signal by changing the frequency of the driving signal from 125 kHz to 116.3 kHz and back to 125 kHz to send a "1" data bit. Carroll et al., col. 7, lines 25-29.

Carroll et al.'s transponder 40 transmits data by Manchester-coded PSK whereby a driving signal has (1) a first phase during the first half of a bit period and a second phase during the second half of a bit period when a "0" is transmitted and (2) the second phase during the first half of a bit period and the first phase during the second half of a bit period when a "1" is transmitted. Carroll et al., col. 20, lines 33-35.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34.

Applicants' claim-64 limitation has to do with applying FSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 64.

Even if the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s PSK circuitry would result in a transponder with the limitations of claim 64 (which it would NOT), there is no motivation for making such a modification.

The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-64 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique.

The examiner has not established *prima facie* obviousness of applicants' claim-64 invention.

CLAIM 65

Claim 65 reads as follows:

65. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-65 limitation has to do with applying FSK/PSK modulation to the PHASE of a driving signal. Thus, McFarlane does not teach the limitation of claim 15.

Carroll et al. utilize a simple PSK technique for communicating data from transponder 40 to controller 10 where the controller 10 is constructed around a commercially-available microcomputer chip. Carroll et al., col. 5, line 64 - col. 6, line 16. The extraction of data from the received signal by transponder 40 is accomplished by the microcomputer chip. Carroll et al., col. 7, lines 12-16. McFarlane discloses a combined FSK/PSK communication technique which involves at the transmit end two frequency multipliers, two phase shifters, logic circuitry, and an analog signal combiner. McFarlane discloses data extraction circuitry at the receive end consisting of two filters, four frequency multipliers, four frequency dividers, two phase detectors, and associated logic circuitry. McFarlane, Fig. 1.

Even if the substitution of McFarlane's FSK/PSK communication circuitry for Carroll et al.'s PSK circuitry would result in a transponder with the limitations of claim 65 (which it would NOT), there is no motivation for making such a modification.

The examiner argues that "it would have been obvious . . . to have used both FSK and PSK simultaneously in the Carroll [*sic*] in order to increase the bandwidth of the system." 08/12/03 Office Action, p. 10. The object in designing communication systems is usually to use less bandwidth to communicate at a certain data rate. And Carroll et al.'s PSK approach is much more efficient in the use of bandwidth than is McFarlane's FSK/PSK approach. *The Communications Handbook*, CRC Press, Inc., Boca Raton, FL (1997), Fig. 19.1. Neither the examiner nor the references provide a reasonable motivation for a person skilled in the art to incorporate McFarlane's FSK/PSK communication technique in Carroll et al.'s invention.

The references do not disclose the claim-65 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique.

The examiner has not established *prima facie* obviousness of applicants' claim-65 invention.

CLAIM 66

Claim 66 reads as follows:

66. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-66 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 66.

The references do not disclose the claim-66 limitation nor do the references provide motivation for making a change in Carroll et al.'s controller 10 modulation technique. Please see discussion under the **CLAIM 65** heading for additional details.

The examiner has not established *prima facie* obviousness of applicants' claim-15 invention.

CLAIM 67

Claim 67 reads as follows:

67. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-67 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this

modulated periodic signal to amplitude modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 67.

The references do not disclose the claim-67 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique. Please see discussion under the **CLAIM 65** heading for additional details.

The examiner has not established *prima facie* obviousness of applicants' claim-67 invention.

CLAIM 68

Claim 68 reads as follows:

68. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

McFarlane's FSK/PSK modulation causes a driving signal to have a frequency of either f_1 or f_2 and one or the other of two phases. McFarlane, col. 4, lines 16-34. Applicants' claim-68 limitation has to do with applying FSK/PSK modulation to a periodic signal and then using this modulated periodic signal to phase modulate the driving signal. Thus, McFarlane does not teach the limitation of claim 68.

The references do not disclose the claim-68 limitation nor do the references provide motivation for making a change in Carroll et al.'s transponder 40 modulation technique. Please see discussion under the **CLAIM 65** heading for additional details.

The examiner has not established *prima facie* obviousness of applicants' claim-68 invention.

XI. WHETHER CLAIMS 36-40 AND 70-80 ARE UNPATENTABLE AS NONSTATUTORY OBVIOUSNESS-TYPE DOUBLE PATENTING WITH RESPECT TO CLAIM 16 OF BEIGEL ET AL. (U.S. 5,235,326) IN VIEW OF CARROLL ET AL. (U.S. 5,517,194).

Claim 16 of Beigel et al. '326 includes the following three limitations:

a means for storing mode control data;

a means for obtaining a measure of the time-dependent absorption of power from said magnetic field by an electronic identification tag, said power absorption measure representing information being communicated by said tag;

a means for extracting said information from said power absorption measure, said information extracting means operating in at least one of a plurality of information extracting modes, each of said information extracting modes defining a specific functional relationship between said information and said time-dependent absorption of power by said tag, said information extracting modes being characterized by said mode control data, the specification of the information extracting mode in said mode control data permitting the extraction of information from said time-dependent absorption of power by said tag.

"The proper question in an obviousness-type double patenting inquiry is whether the claims at issue would have been obvious to one of ordinary skill in the art over the subject matter of the claims in the first patent. See, e.g., In re Kaplan, 789 F.2d 1574, 1579-80, 229 USPQ 678, 682 (Fed. Cir. 1986); In re Longi, 759 F.2d 887, 893, 225 USPQ 645, 648 (Fed. Cir. 1985). 'In considering the question, the patent disclosure may not be used as prior art.' In re Vogel, 422 F.2d 438, 441, 164 USPQ 619, 622 (CCPA 1970). Fed. R. Civ. P. 52(a); Longi, 759 F.2d at 893, 225 USPQ at 648." ***Research Corporation Technologies, Inc. v. Gensia Laboratories, Inc.*****, No. 00-1166 (Fed. Cir. 03/23/2001), 2001.CFC.0000177 par. 32 <http://www.versuslaw.com>**

CLAIMS 36-40

The invention protected by patent '326 is a "multi-mode identification system" which is capable of (1) generating a magnetic field at a plurality of frequencies and (2) extracting information in accordance with a plurality of protocols, thereby permitting the reader to be used with tags of different designs and made by different manufacturers. '326 Abstract.

The claim-16 limitations are focused on protecting the structure of a reader which is capable of operating as a multi-mode identification system. Claim 16 includes the limitation "a means for generating a reversing magnetic field" which is a necessary component of short-range identification systems but not new or novel at the time the '326 application was filed.

Claims 36-40 of the present application are focused on new and novel structures for generating "reversing magnetic fields". New and novel structures for implementing a necessary and well-known means-plus-function limitation cannot be interpreted as an obvious modification to make in the '326 invention.

CLAIMS 70-71, 74-80

Claims 70 and 71 have to do with methods of interrogating a tag whereby a bit-timing clock signal is embedded in an alternating magnetic field. The only point of commonality between claim 16 of patent '326 and claims 70-71 is the necessary and well-known reversing (or alternating)

magnetic field. There is nothing in claim 16 to suggest the use of an embedded bit-timing clock signal in the reversing magnetic field.

Claims 74 and 75 have to do with methods for responding to an interrogation wherein a bit-timing clock signal is embedded in the alternating magnetic field. There is nothing in claim 16 concerning an interrogation which embeds a bit-timing clock signal in a reversing magnetic field, and there is nothing concerning the use of such a bit-timing clock signal in responding to such an interrogation.

Claims 76 and 77 have to do with methods of communication between and interrogator and a responder wherein a bit-timing clock signal is embedded by the interrogator in an alternating magnetic field. There is nothing in claim 16 concerning an interrogation which embeds a bit-timing clock signal in a reversing magnetic field, and there is nothing concerning the use of such a bit-timing clock signal in a response to such an interrogation.

Claims 74 and 77 also have limitations having to do with the use of "weighted integrations" of the received signal using the bit-timing clock signal. There is nothing in claim 16 suggesting the use of weighted integrations in extracting data from signals.

Claims 78, 79, and 80 are for apparatus for practicing respectively the methods of claims 73, 76, and 77. The conclusions concerning claims 73, 76, and 77 also apply to claims 78, 79, and 80.

CLAIMS 72

Claim 72 has to do with a method of extracting a message containing a sync sequence from a communication from a tag. Because the message is continually repeated in the communication and

because the communication may contain "false-sync" sequences, there is some difficulty in determining where a message starts.

Claim 16 of patent '326 includes a limitation having to do with extracting information from tags of different designs using different information extracting modes. There is nothing in this limitation (or any of the other limitations of claim 16) which suggest the method of claim 72.

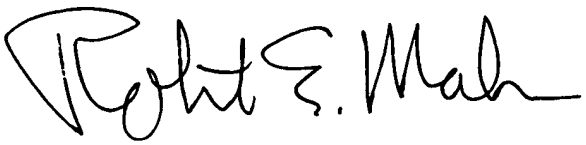
CLAIM 73

Claim 73 has to do with a method for responding to an interrogation be a reader whereby a resonating circuit used to receive the interrogation is maintained in resonance. Claim 73 pertains to a tag while claim 16 of patent '326 has to do with a reader. There is nothing in claim 16 that suggests that the resonating circuit used in a tag should be maintained in resonance.

* * * * *

Claims 1-80 appear to be in condition for allowance and such action is respectfully requested.

Respectfully submitted,



Date: October 27, 2003
Telephone: (310) 459-8728

Robert E. Malm
Reg. No. 34,662